Unleashing Growth in EDA with Pioneering Innovations

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GM and Corp Staff, EDA Group

SYNOPSYS®

Our Technology, **Your Innovation**™

Synopsys Cautionary Statement Regarding Forward Looking Statements

This presentation contains certain forward-looking statements within the meaning of the federal securities laws with respect to the proposed transaction between Synopsys and Ansys, including, but not limited to, statements regarding the proposed transaction; the anticipated market demand and outlook, products and business lines of Synopsys, Ansys and the combined company, and the benefits of and cost and revenue synergies from the proposed transaction to Synopsys; combined company financial information; long-term leverage and debt paydown targets; short-term and long-term financial targets of Synopsys, Ansys and the combined company; Synopsys' expectations and objectives; strategies related to Synopsys' and Ansys' products, technology and services; market, software, opportunities, strategies and technological trends and their potential impacts on total addressable markets, products and business lines, such as artificial intelligence; customer demand and market expansion of each of Synopsys and Ansys and the combined company; Synopsys' planned product releases and capabilities; industry growth rates; the current and projected total addressable markets of Synopsys and certain of its segments, Ansys and the combined company; and Synopsys' plans to divest its Software Integrity Group ("SIG") segment. These forward-looking statements generally are identified by the words "believe," "project," "expect," "anticipate," "estimate," "intend," "strategy," "future," "opportunity," "plan," "may," "should," "will," "would," "will be," "will continue," "will likely result," and similar expressions or the negatives of these words or other comparable terminology to convey uncertainty of future events or outcomes. Forward-looking statements are predictions, projections and other statements about future events that are based on current expectations and assumptions and, as a result, are subject to risks and uncertainties.

Many risks, uncertainties and other factors could cause actual future events to differ materially from any future results, performance or achievements expressed or implied by the forward-looking statements, including, but not limited to: (i) the completion of the proposed transaction on anticipated terms and timing, anticipated tax treatment and unforeseen liabilities, future capital expenditures, revenues, expenses, earnings, synergies, economic performance, indebtedness, financial condition, losses, pricing trends, future prospects, credit ratings, business and management strategies which may adversely affect each of Synopsys' and Ansys' business, financial condition, operating results and the price of their common stock, (ii) the failure to satisfy the conditions to the consummation of the proposed transaction, including the adoption of the merger agreement by the stockholders of Ansys and the receipt of certain governmental and regulatory approvals on the terms expected, in a timely manner, or at all, (iii) the risk that such regulatory approvals may result in the imposition of conditions that could adversely affect, following completion of the proposed transaction (if completed), the combined company or the expected benefits of the proposed transaction (including as noted in any forward-looking financial information), (iv) uncertainties as to access to available financing (including any future refinancing of Ansys' or the combined company's debt) to consummate the proposed transaction upon acceptable terms and on a timely basis or at all, (v) the occurrence of any event, change or other circumstance that could give rise to the termination of the merger agreement, (vi) the effect of the announcement or pendency of the proposed transaction on Ansys' or Synopsys' business relationships, competition, business, financial condition, and operating results, (vii) risks that the proposed transaction disrupts current plans and operations of Ansys or Synopsys and the ability of Ansys or Synopsys to retain and hire key personnel, (viii) risks related to diverting either management team's attention from ongoing business operations of Ansys or Synopsys, (ix) the outcome of any legal proceedings that may be instituted against Ansys or Synopsys related to the merger agreement or the proposed transaction, (x) the ability of Synopsys to successfully integrate Ansys' operations and product lines, (xi) the ability of Synopsys to implement its plans, forecasts, expected financial performance and other expectations with respect to Ansys' business or the combined business after the completion of the proposed mergers and realize the benefits expected from the proposed transaction (if completed) as well as manage the scope and size of the combined company, (xii) the ability of Synopsys to manage additional debt and debt covenants as well as successfully de-lever following the proposed transaction and the outcome of any strategic review and any resulting proposed transactions, (xiii) risks associated with third party contracts containing consent and/or other provisions that may be triggered by the proposed transaction, (xiv) uncertainty in the macroeconomic environment and its potential impact on the semiconductor and electronics industries, (xv) uncertainty in the growth of the semiconductor, electronics and artificial intelligence industries, (xvi) the highly competitive industries Synopsys and Ansys operate in, (xvii) actions by the U.S. or foreign governments, such as the imposition of additional export restrictions or tariffs, (xviii) consolidation among Synopsys' customers and within the industries in which Synopsys operates, as well as Synopsys' dependence on a relatively small number of large customers, (xix) the evolving legal, regulatory and tax regimes under which Ansys and Synopsys operate and (xx) restrictions during the pendency of the proposed transaction that may impact Ansys' or Synopsys' ability to pursue certain business opportunities or strategic transactions. The foregoing list of risks, uncertainties and factors is not exhaustive. Unlisted factors may present significant additional obstacles to the realization of forward-looking statements.

You should carefully consider the foregoing factors and the other risks and uncertainties that affect the businesses of Synopsys and Ansys described in the "Risk Factors" section of their respective Annual Reports on Form 10-K, Quarterly Reports on Form 10-Q and other documents filed by either of them from time to time with the SEC, including Synopsys' registration statement on Form S-4 (File No. 333-277912) with the SEC on March 14, 2024. These filings identify and address other important risks and uncertainties that could cause actual events and results to differ materially from those contained in the forward-looking statements. Forward-looking statements speak only as of the date they are made. All forward-looking statements by their nature address matters that involve risks and uncertainties, many of which are beyond Synopsys' and Ansys' control, and are not guarantees of future results. Readers are cautioned not to put undue reliance on forward-looking statements, and Synopsys and Ansys assume no obligation and do not intend to update or revise these forward-looking statements, whether as a result of new information, future events, or otherwise, unless required by law. Neither Synopsys nor Ansys gives any assurance that either Synopsys or Ansys will achieve its expectations.

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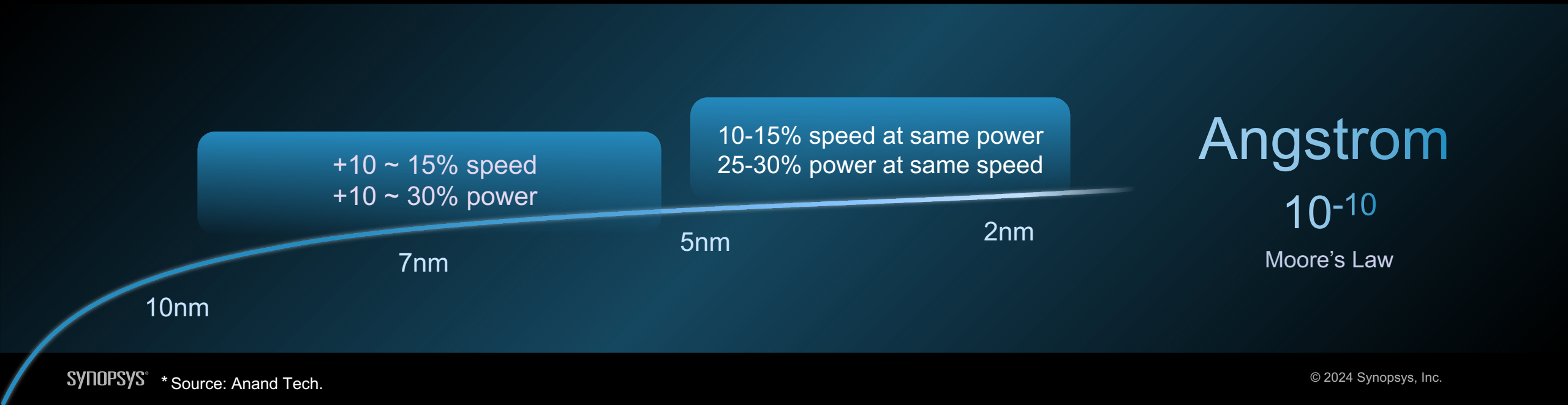
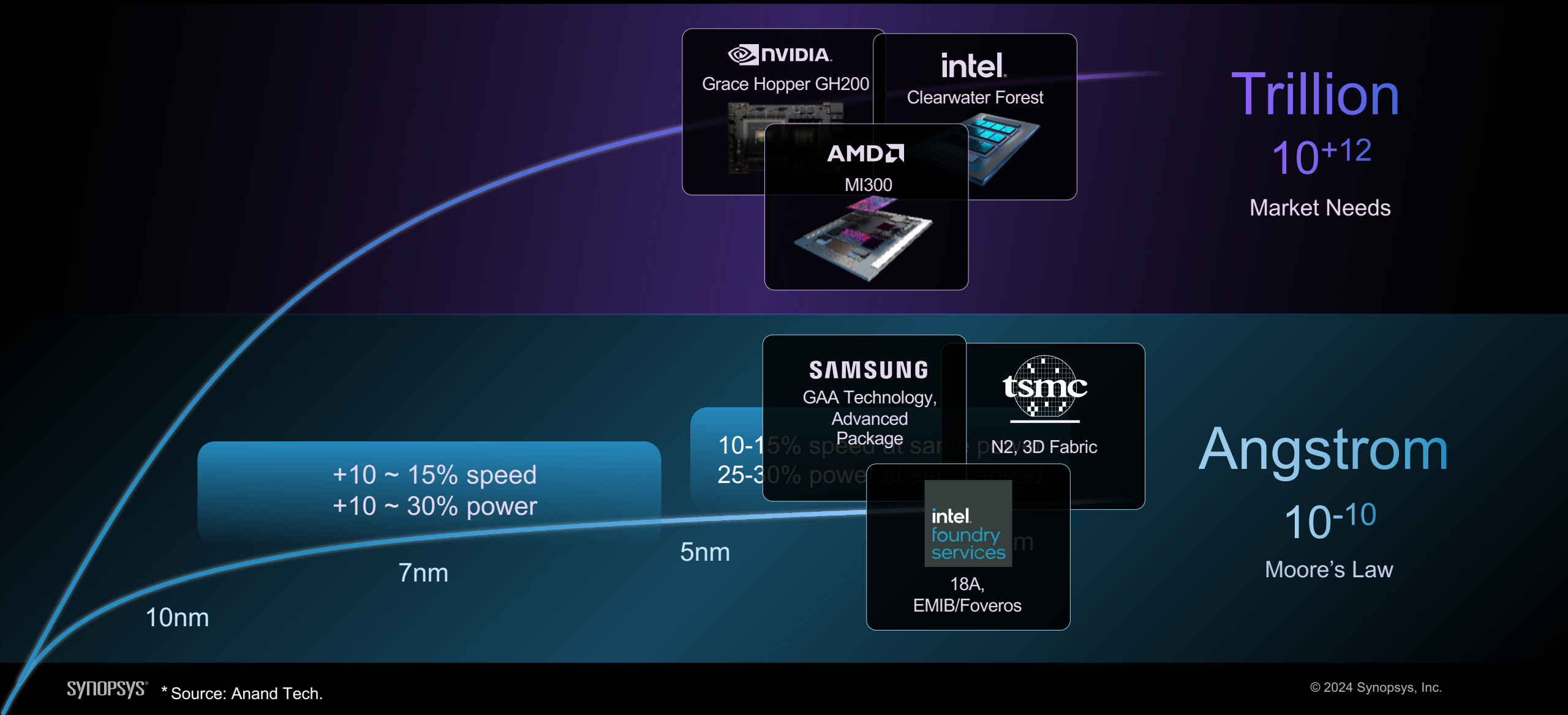
Synopsys EDA is Moving from Important to Mission Critical

Process Scaling Gains Lagging Compute Growth Needs



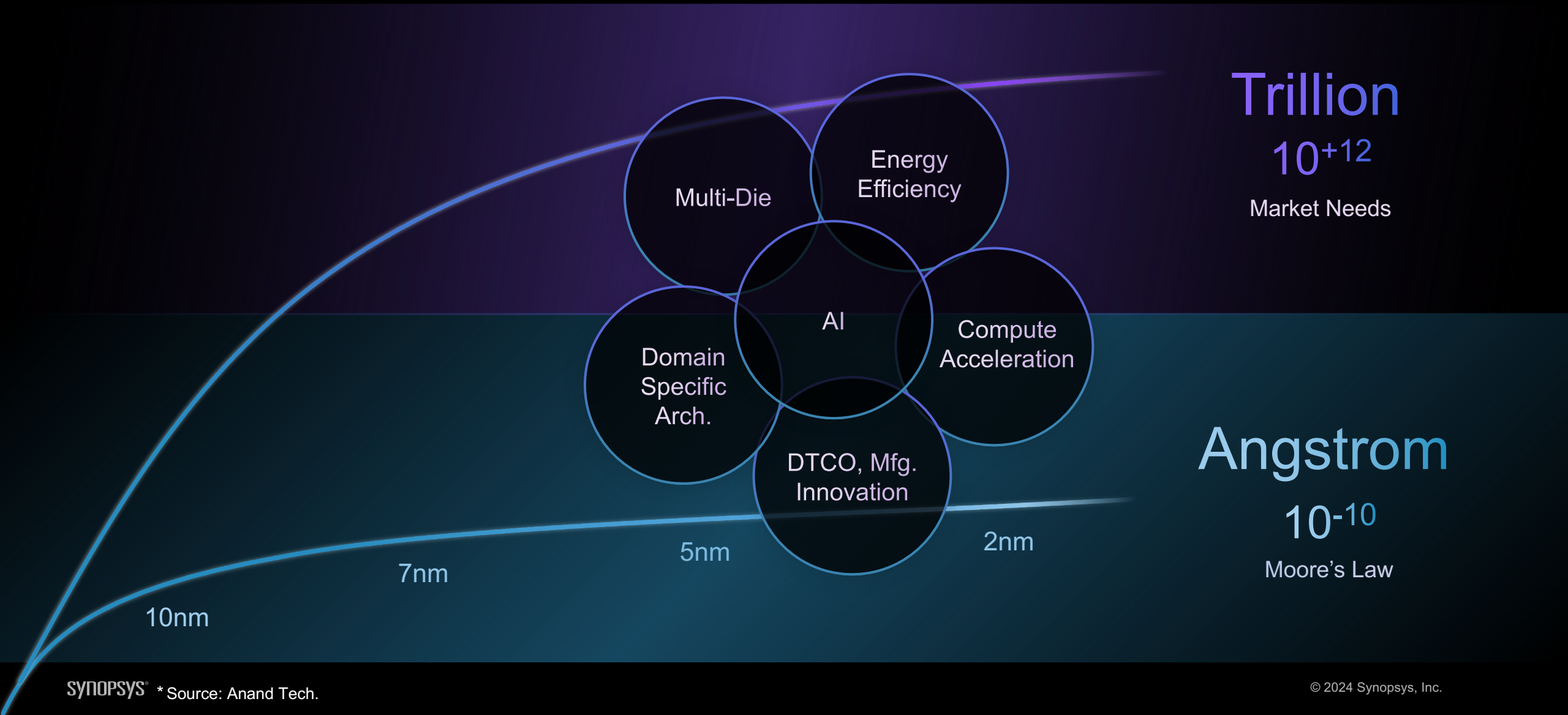
SYNOPSYS® * Source: Anand Tech.

Process Scaling Gains Lagging Compute Growth Needs



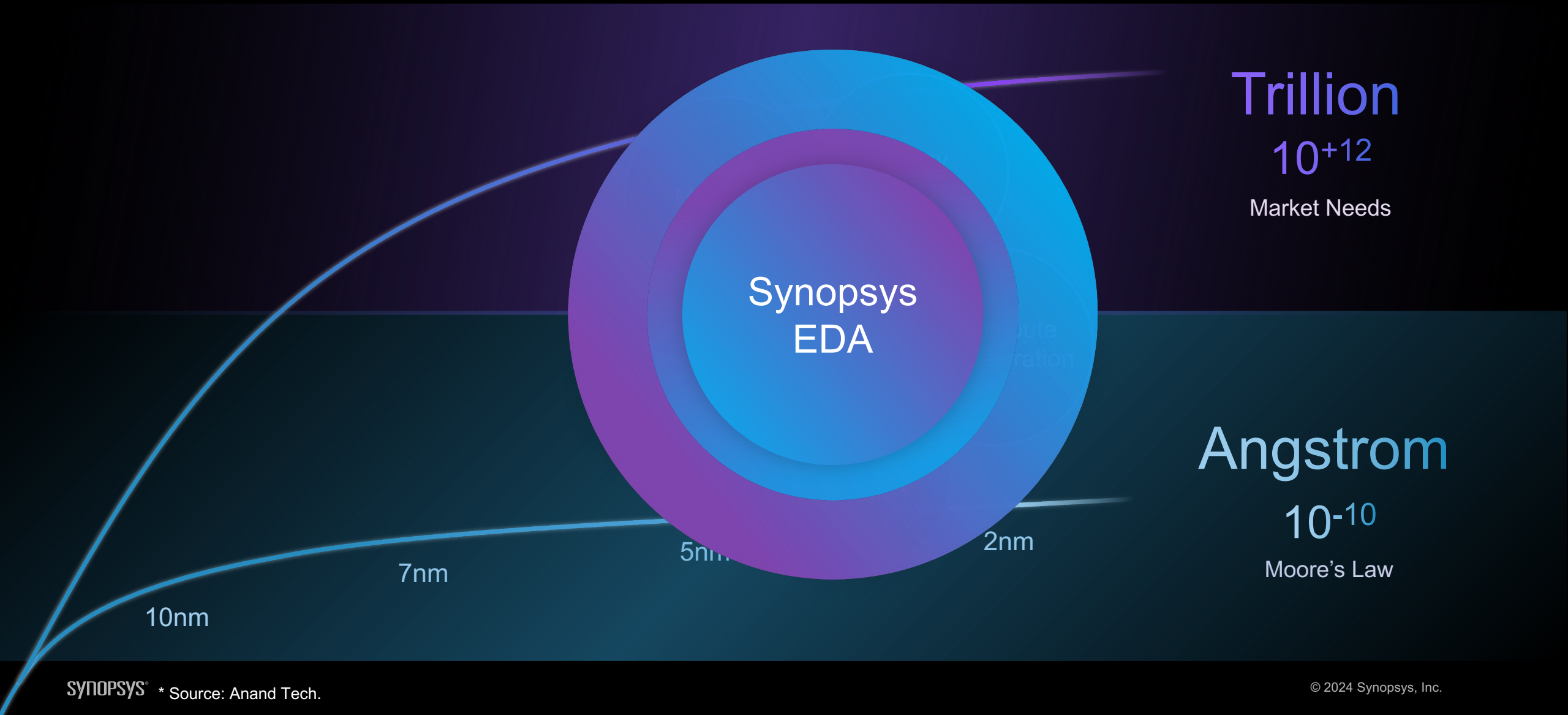
SYNOPSYS® * Source: Anand Tech.

Multiple Innovations Closing the Gap



SYNOPSYS® * Source: Anand Tech.

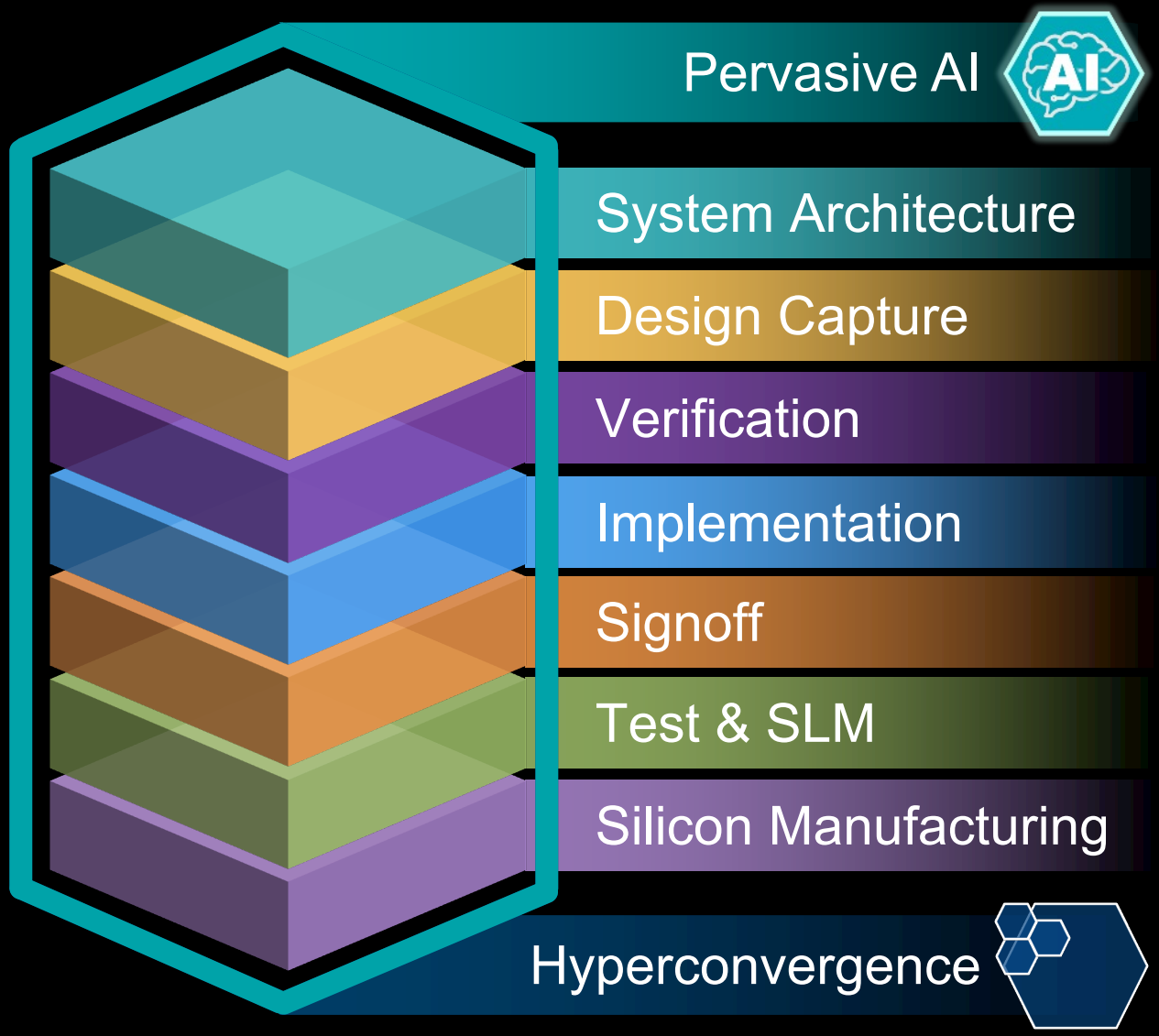
Synopsys is Mission Critical to Enabling these Innovations



SYNOPSYS® * Source: Anand Tech.

Synopsys EDA Well Positioned with Breadth and Depth of Portfolio

AI-Powered Full-Stack EDA Portfolio



- #1 in EDA, 30+ years of EDA investment
- 65% of Synopsys FY23 revenue
- Leader in Digital Design and Verification
- Leader in GPU-Accelerated Analog Verification
- Gold Standard in Signoff and TCAD
- Pioneer in Silicon Lifecycle Management

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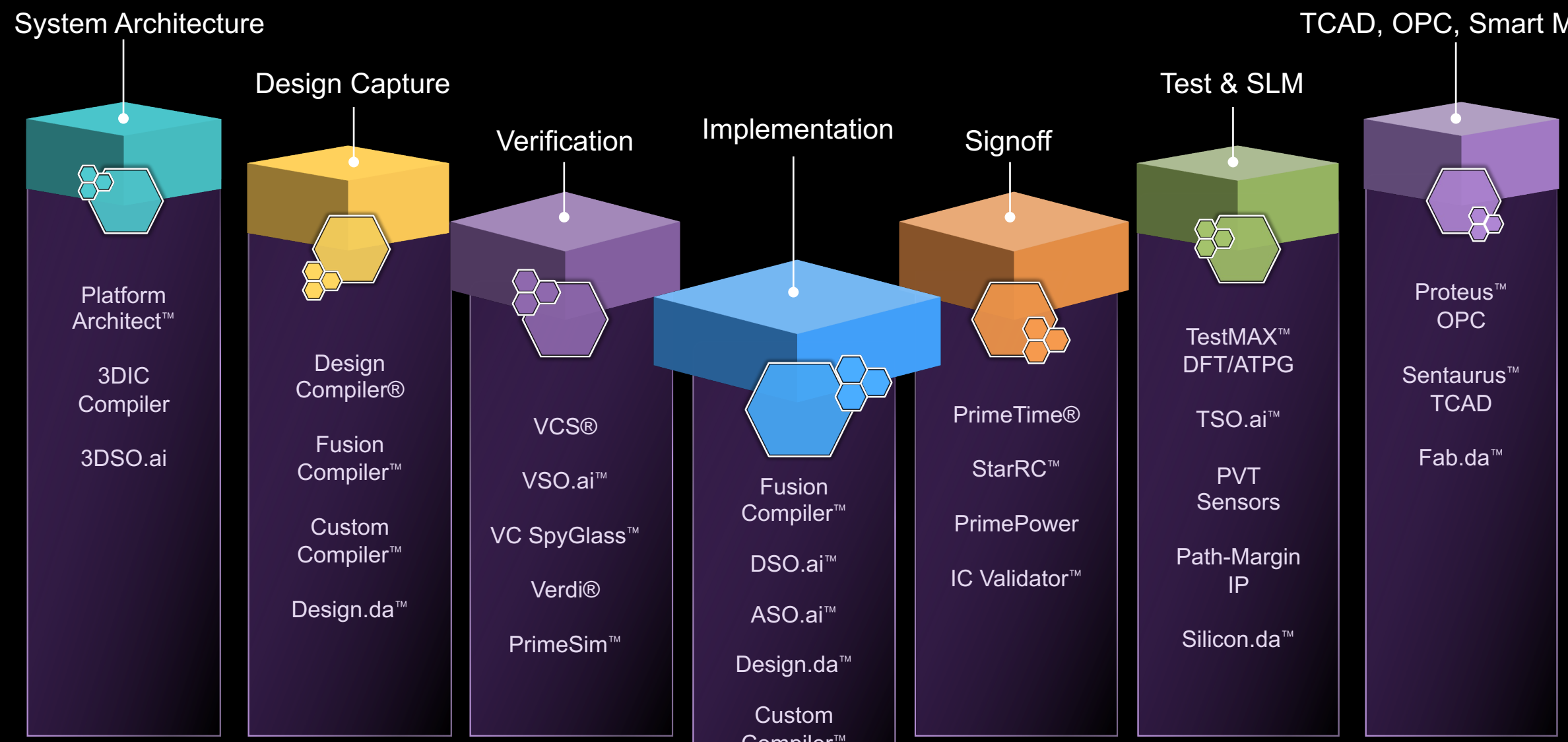
Industry-Leading EDA Products



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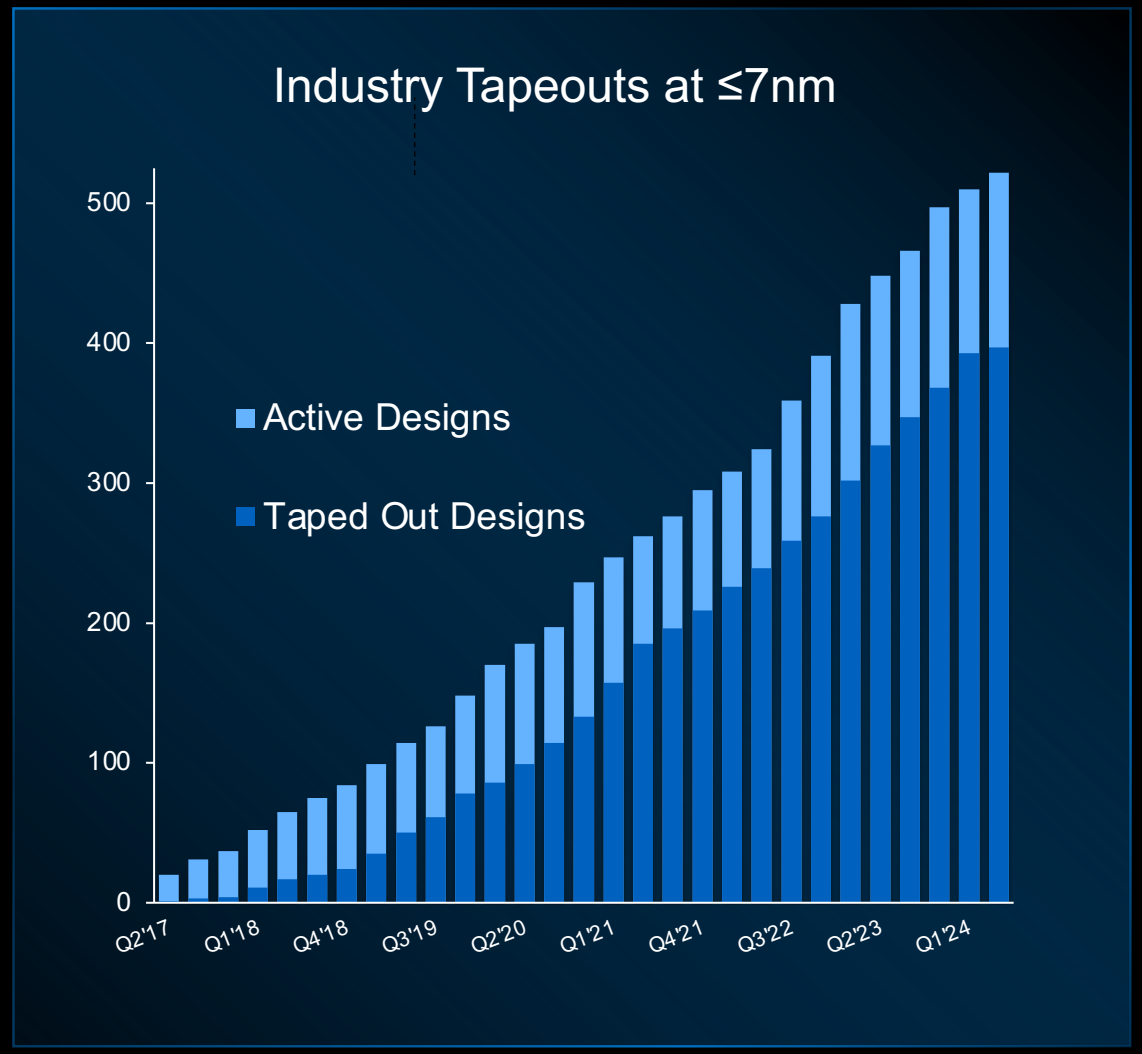
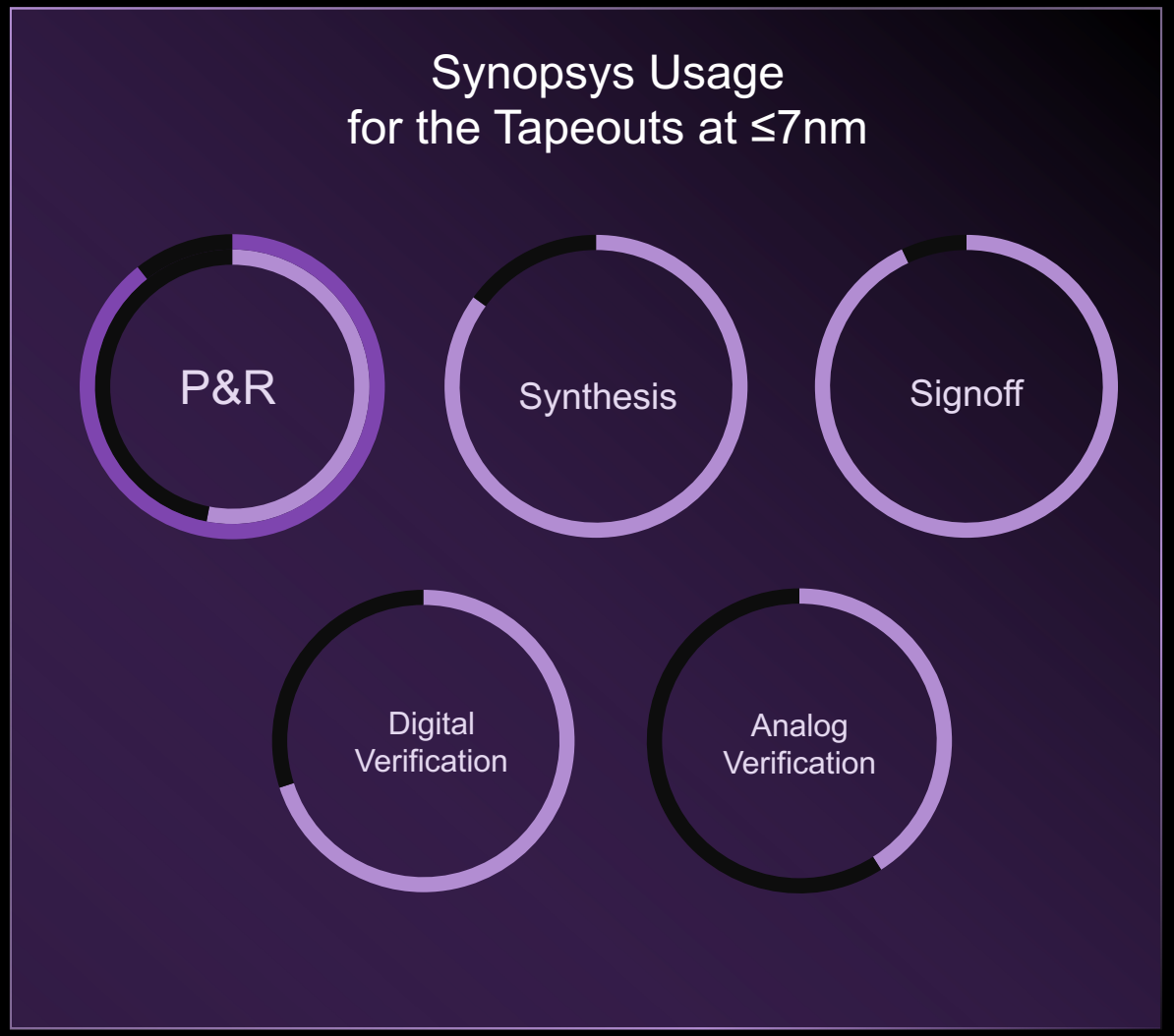
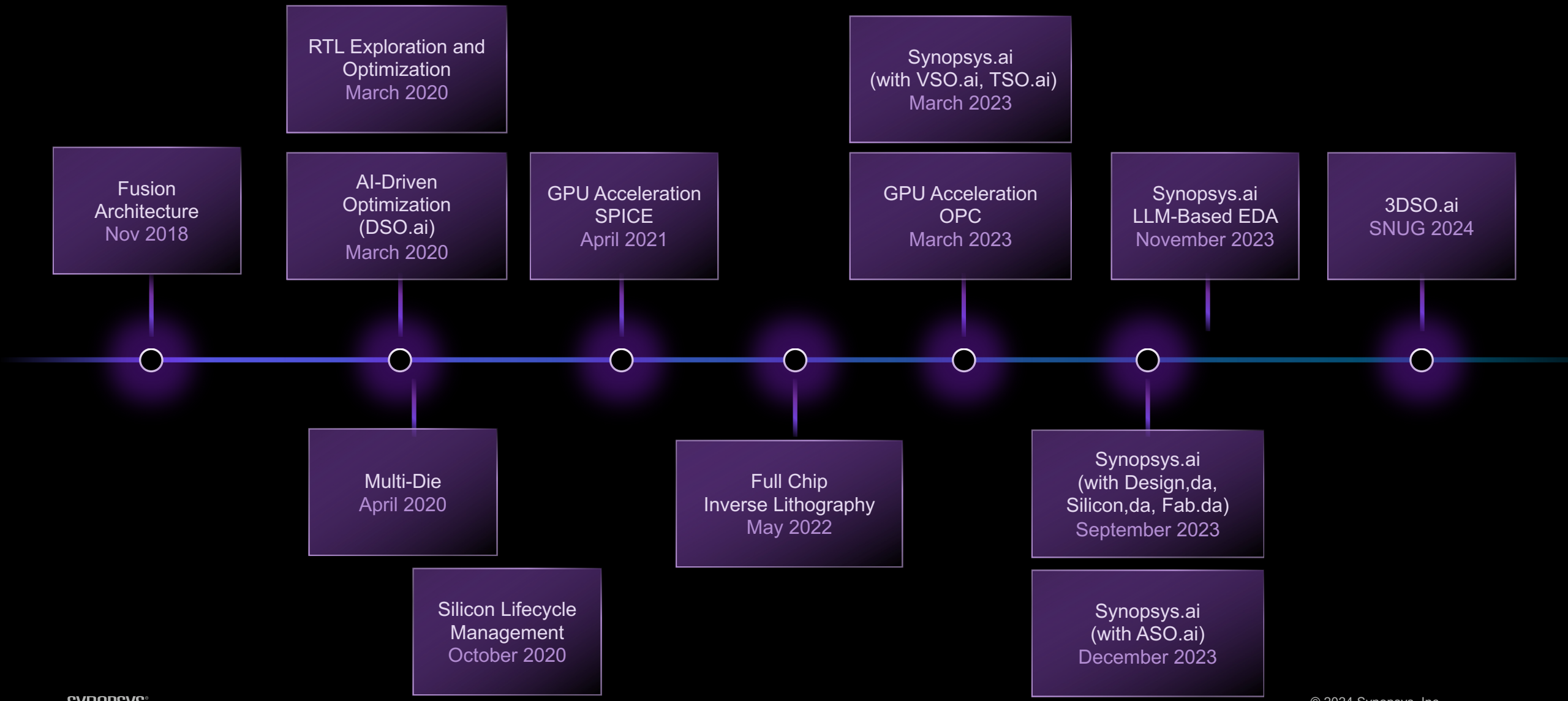
Preferred Choice for Established and Emerging Nodes



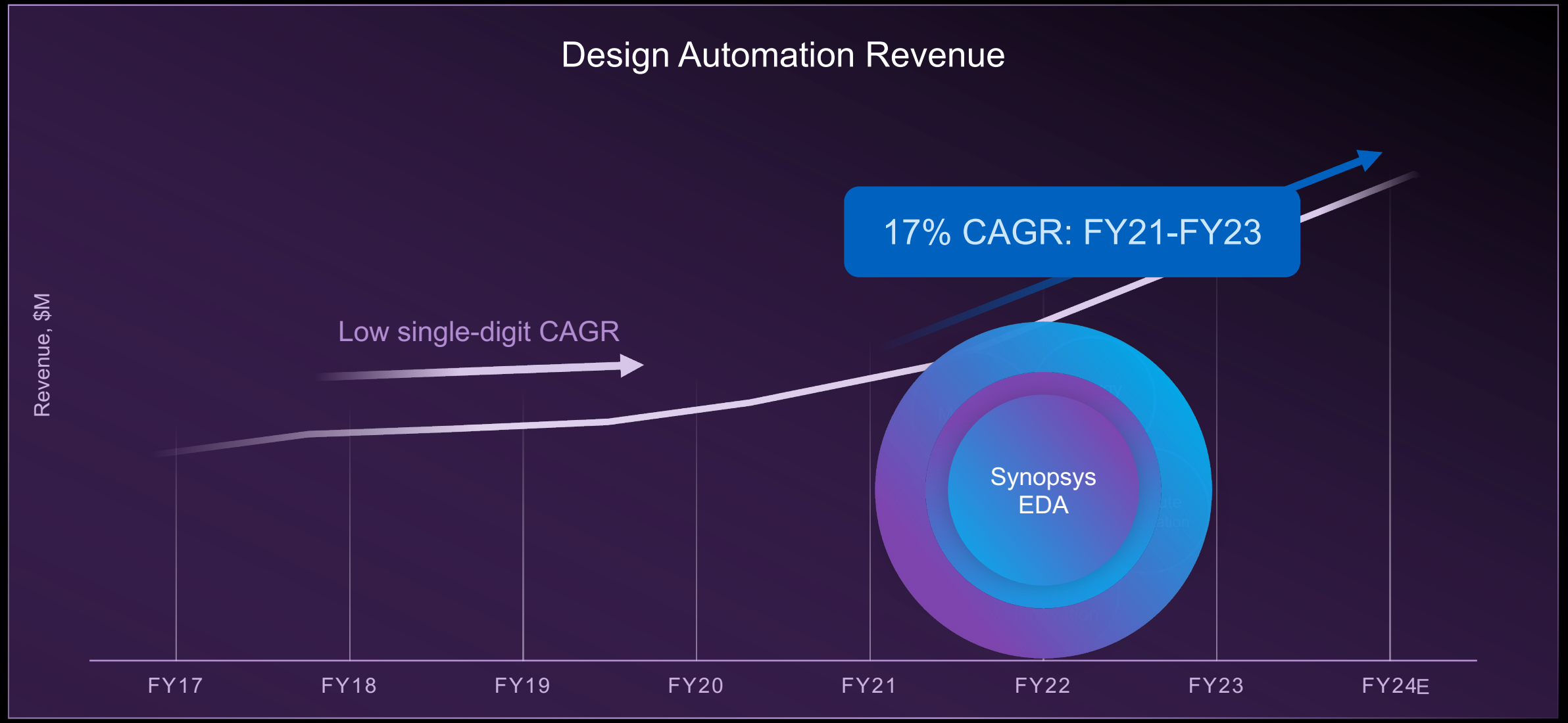


Source: Synopsys Global Technical Services, February 2024

Pioneering Innovations Enable Semiconductor Progress

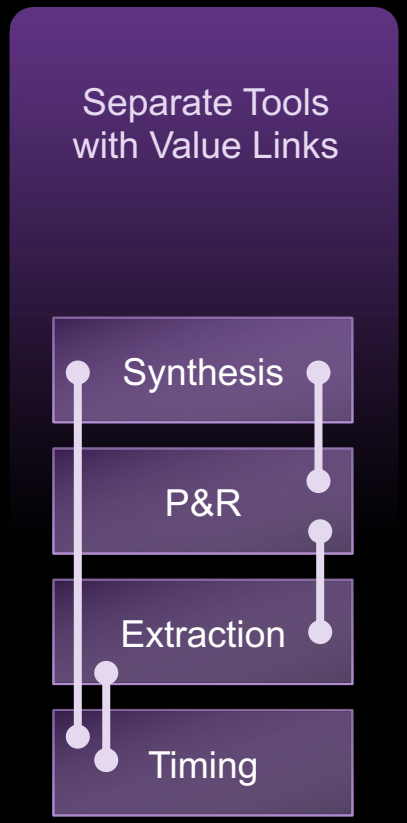


Delivering Strong Double-Digit Growth



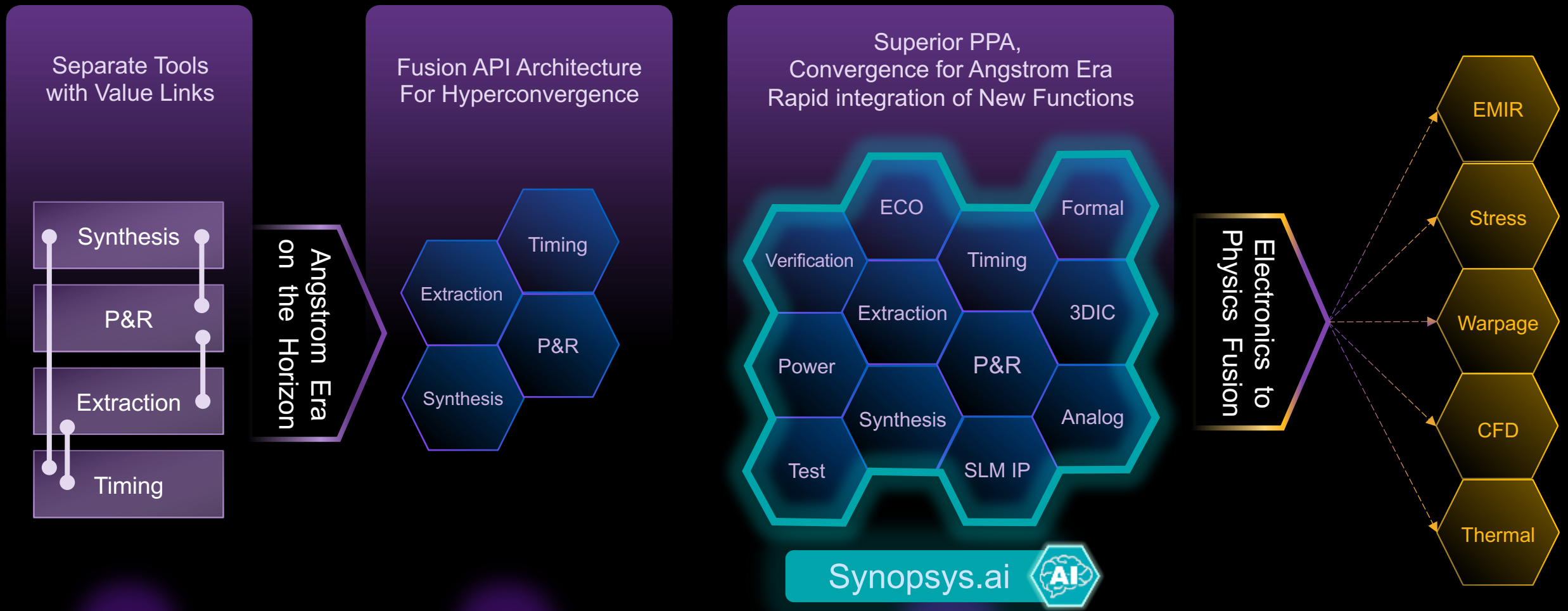
It’s All About the Architecture

Synopsys Next-Gen Fusion EDA Architecture



Pre 2016

Synopsys Next-Gen Fusion EDA Architecture



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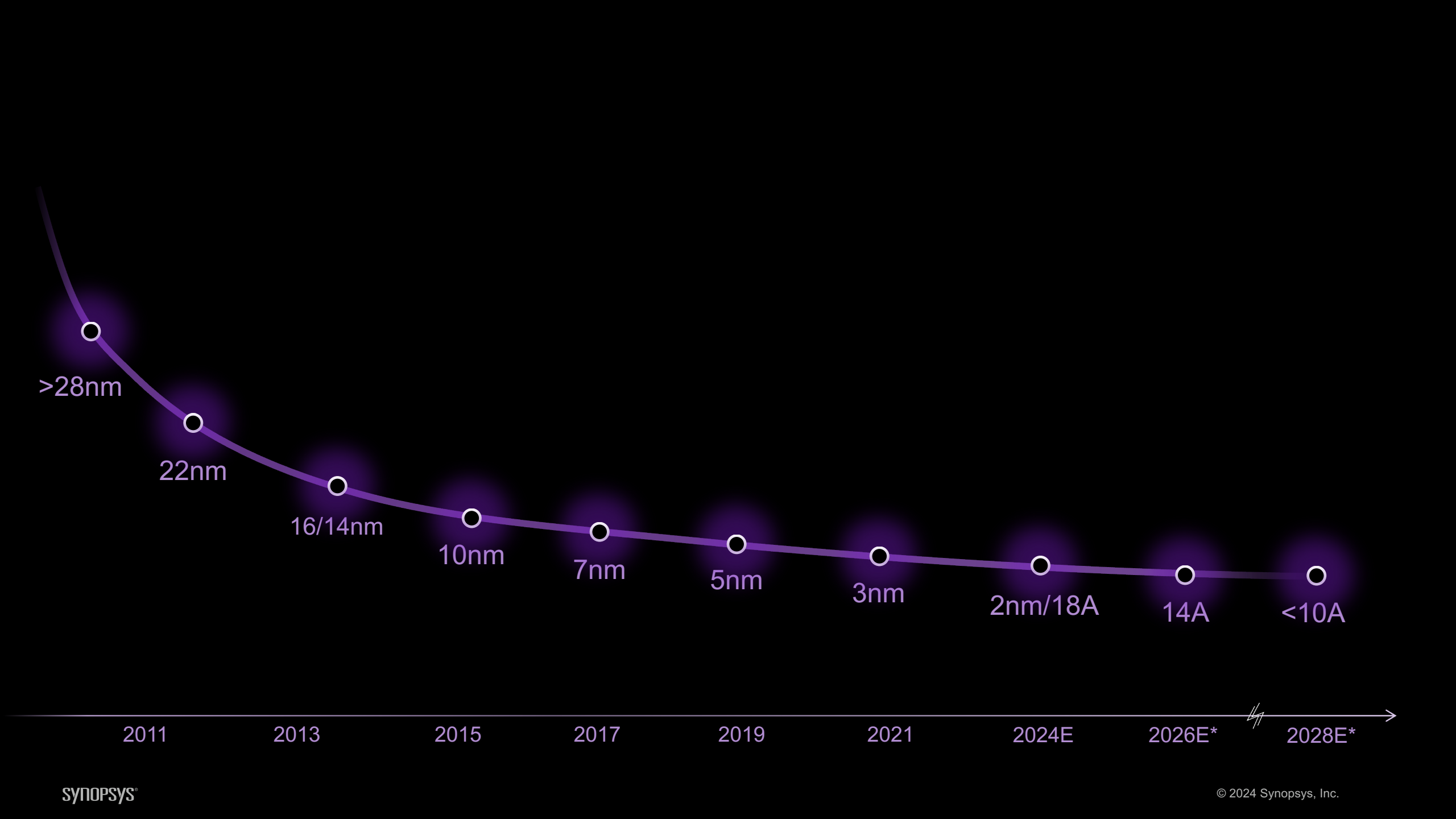
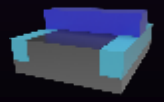
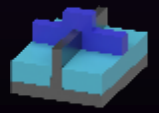
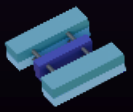
Pioneering Innovations Unleash New Growth Vectors

March to Angstroms



Maximizing Process Entitlement in Angstrom Era

Library	PPA Optimized	Double Patterning	Nanosheet Optimized	Pre-PDK DTCO
P&R	Double Patterning	Hybrid Row	Backside Power	Backside Clock, Signal
Signoff	SI Modeling	Hierarchical Modeling	Variability Modeling	Hybrid Extraction
Mask	Model Based OPC	Inverse Lithography (ILT)	Curve OPC	High NA EUV
	λ 248nm	Deep UV = 193nm, 193i		Extreme UV = 13.5nm
TCAD DTCO	 Planar	Physics based modeling	 FinFET	3D simulation
	 GAA	New materials, DTCO	 CFET	2D materials

Maximizing Process Entitlement in Angstrom Era

Library	**Foundation Libraries**
P&R	**Fusion Compiler**
Signoff	**Prime* (Time, Power, Simulation, ECO)**
Mask	**Proteus OPC**
TCAD DTCO	**Sentaurus**

Highest PPA Delivered at 2nm/18A

From All Leading Foundries with the Synopsys Portfolio

Maximizing Process Entitlement in Angstrom Era

TSMC and Synopsys help our mutual customers achieve the best-in-class design results across the full Synopsys EDA stack on TSMC's most advanced N2 process

Dan Kochpatcharin
Head of Design Infrastructure Management Division, TSMC

Synopsys provides designers with access to industry-leading certified EDA flows and IP that deliver the best performance, power, and area for the Intel 18A technology

Rahul Goyal
Vice President & General Manager, Product & Design Ecosystem, Intel Foundry

…our latest, advanced 3nm GAA process has benefited from our extensive collaboration with Synopsys to enable the efficient realization of the process' promise.

Sangyun Kim
Vice President of Foundry Design Technology Team, Samsung Electronics

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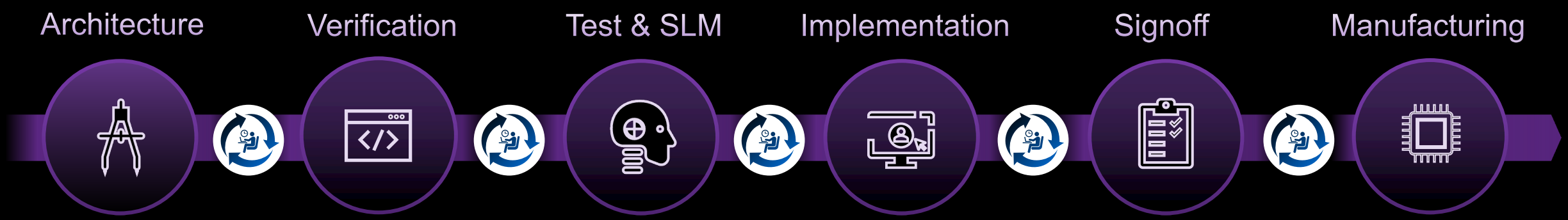
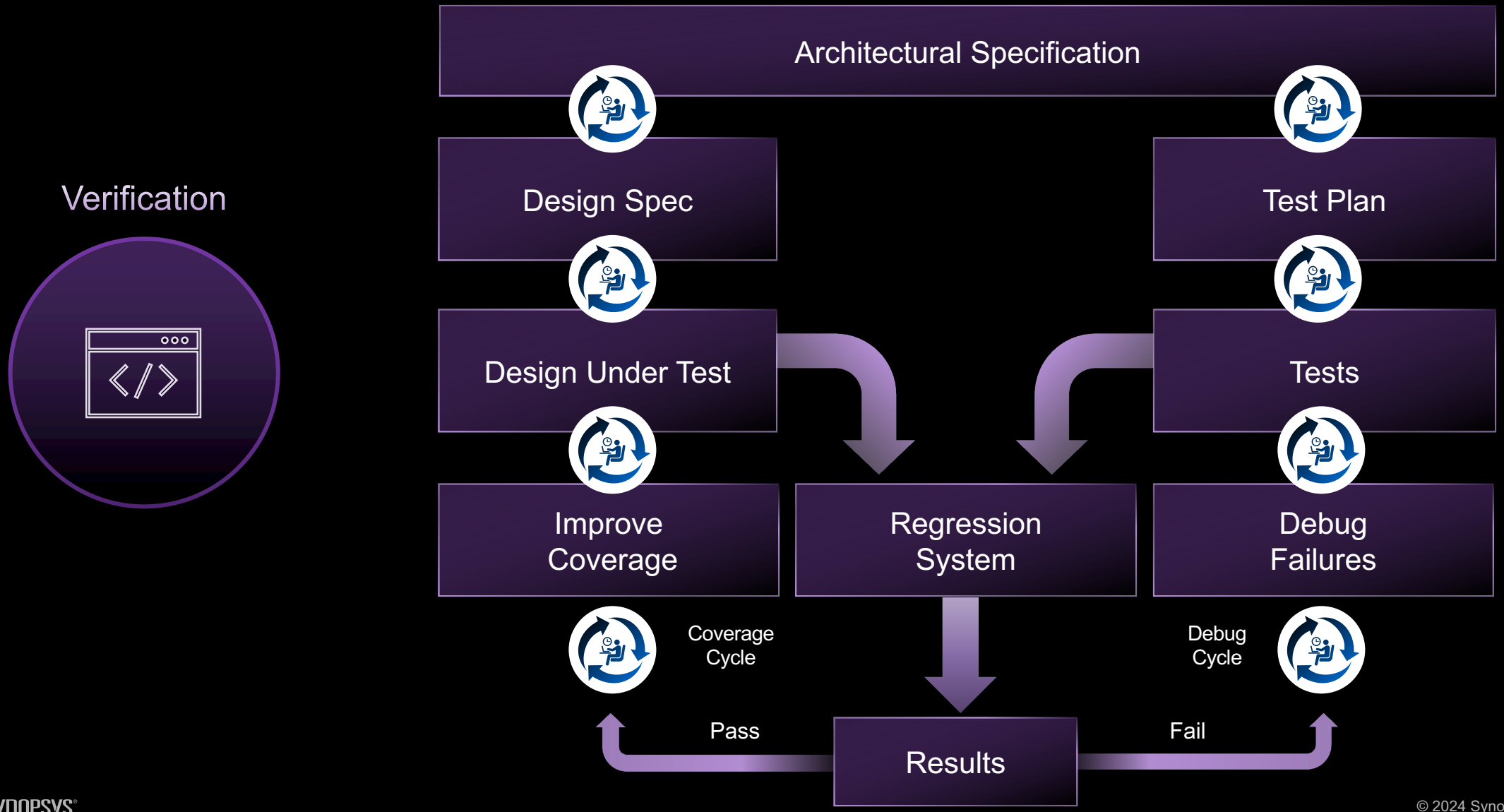
Pioneering Innovations Unleash New Growth Vectors

Synopsys.ai

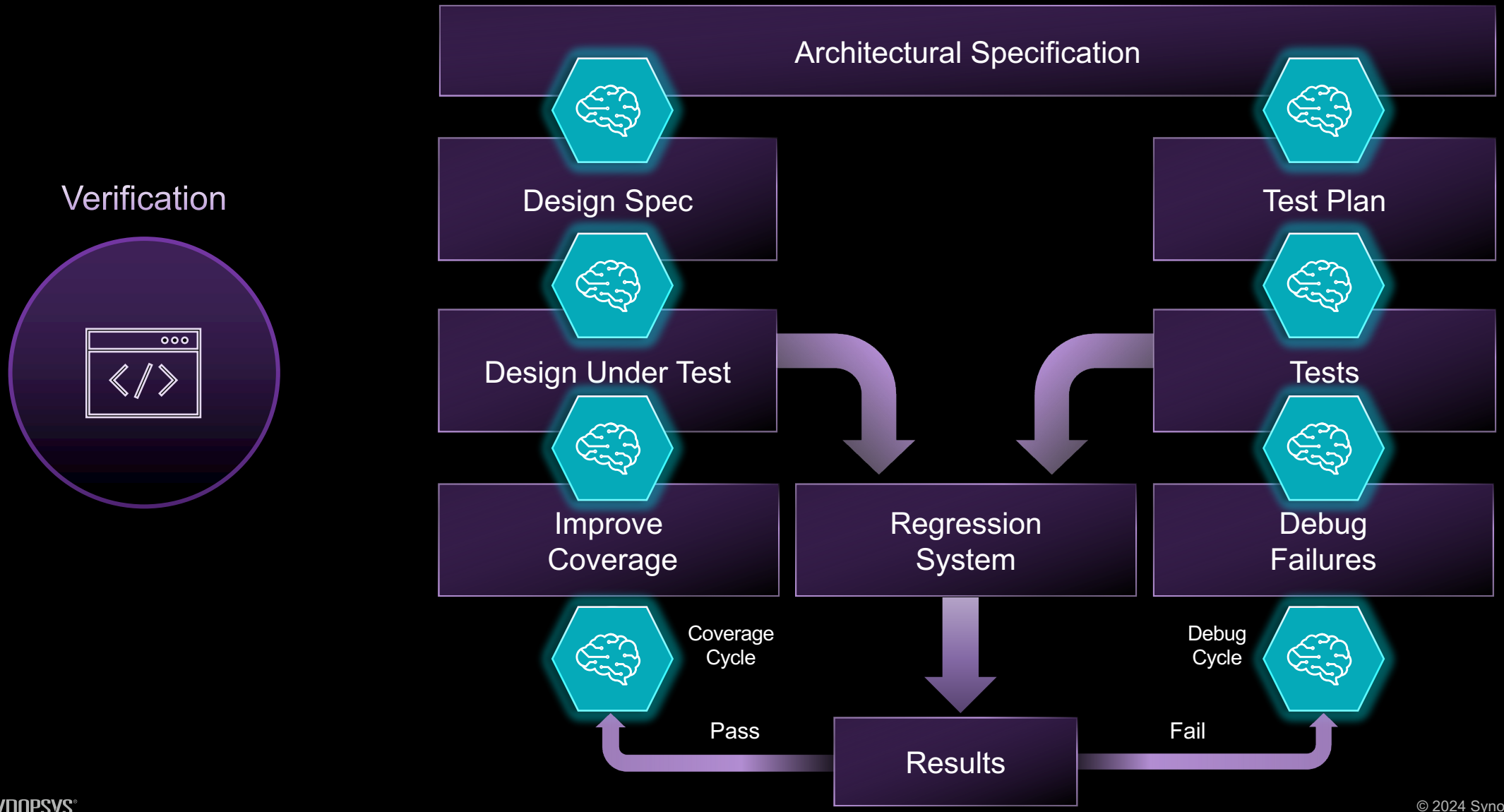
EDA Workflow Offers Opportunities for AI



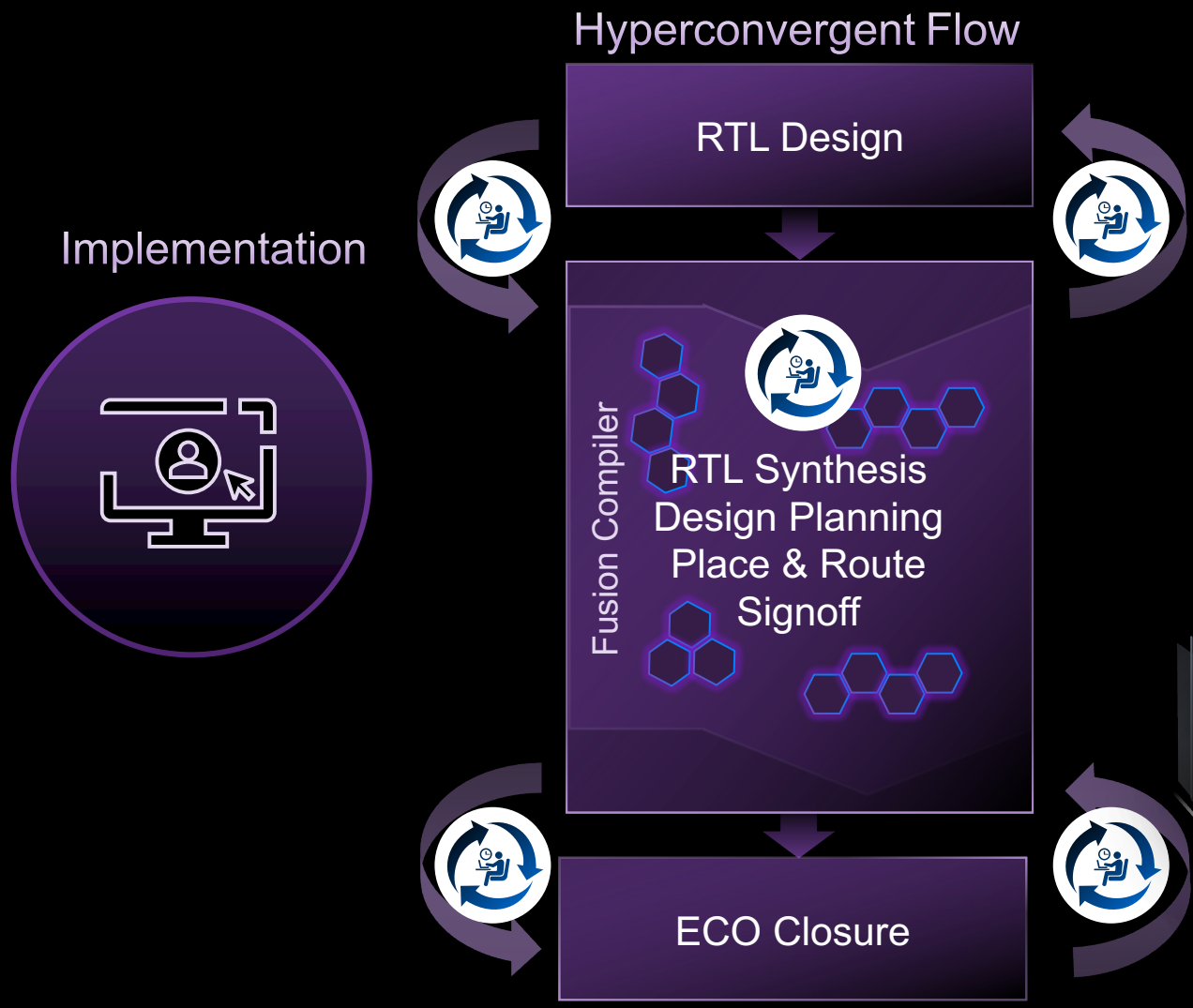
EDA Workflow Offers Opportunities for AI

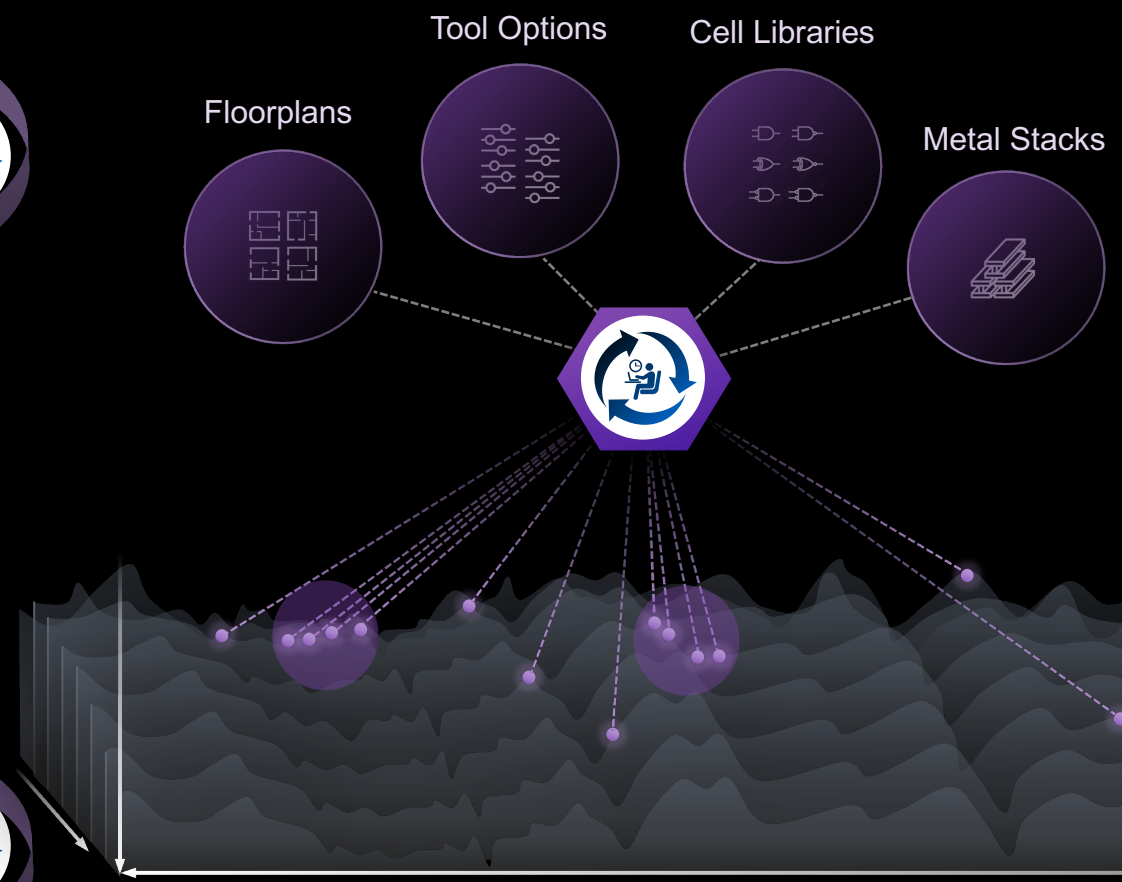


EDA Workflow Offers Opportunities for AI

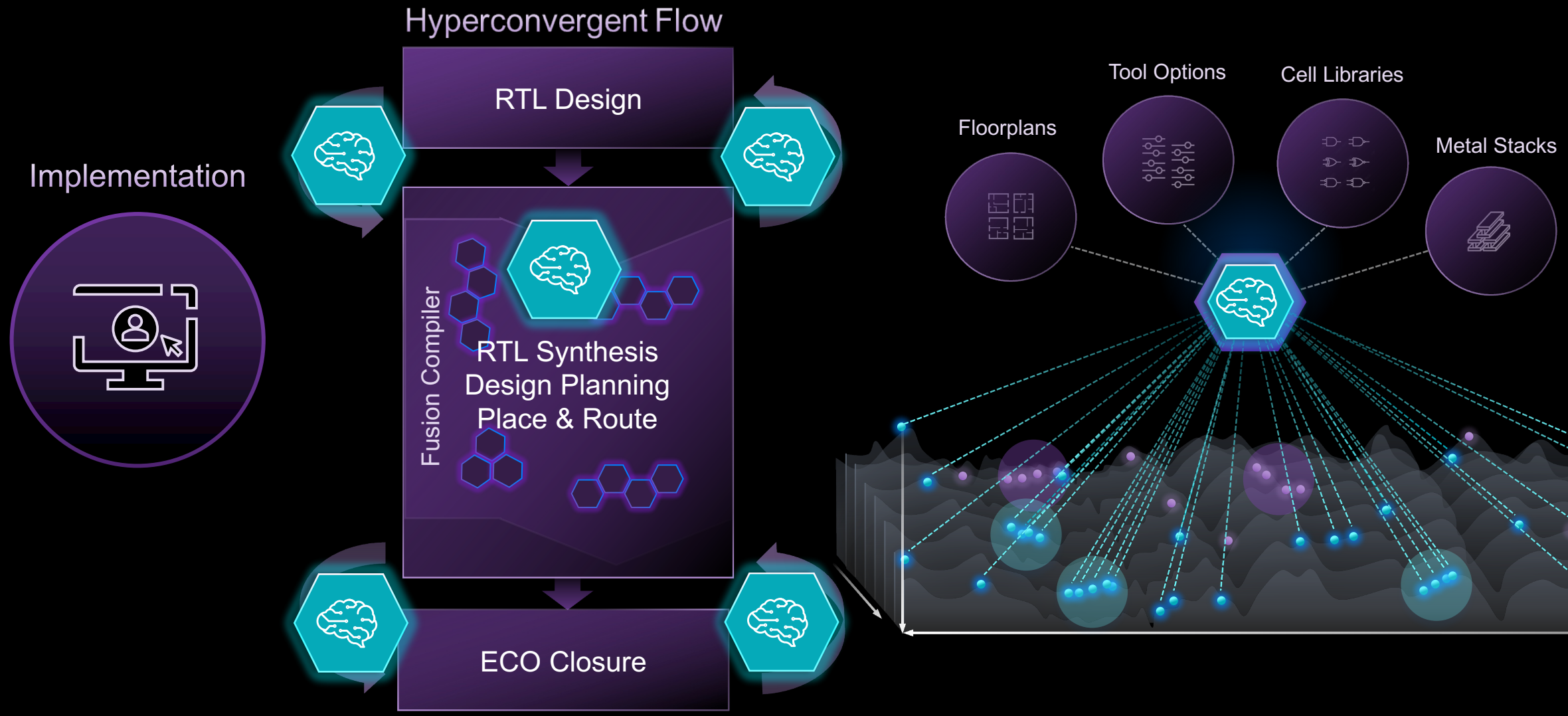


EDA Workflow Offers Opportunities for AI

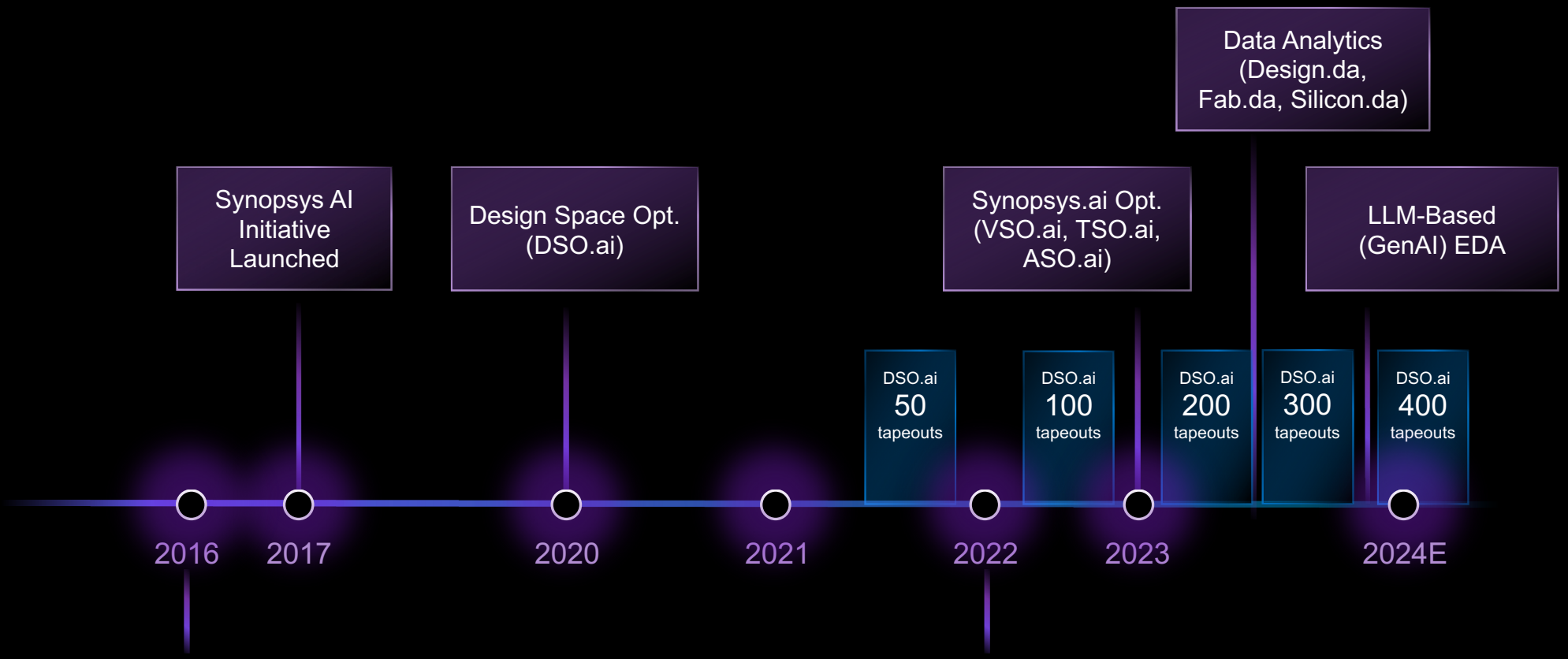


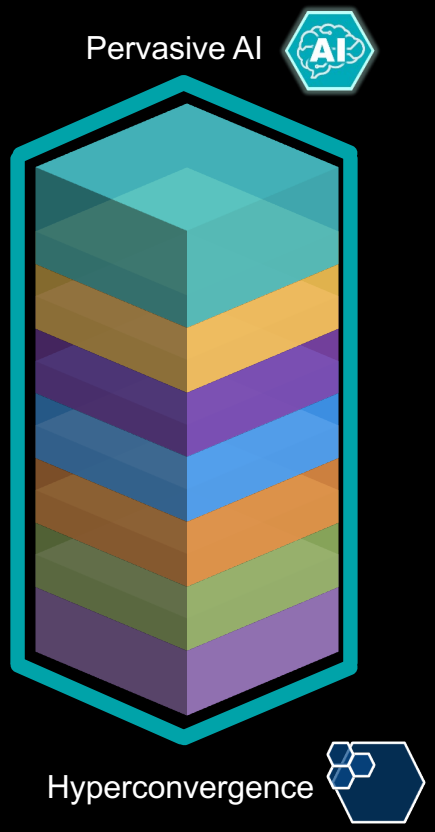


EDA Workflow Offers Opportunities for AI



Blistering Pace of AI Innovations





SYNOPSYS®

Market Leaders Realizing Significant Gains from Synopsys.ai

DSO.ai*

28nm Image sensor	12% Area Shrink	4nm Mobile SoC	25% Lower Power	FinFET CPU	20% Faster TAT
7nm Automotive CPU	3X Productivity	5nm HPC	4.5% Fmax Boost	6nm Mobile	6.5% Smaller Area

VSO.ai*

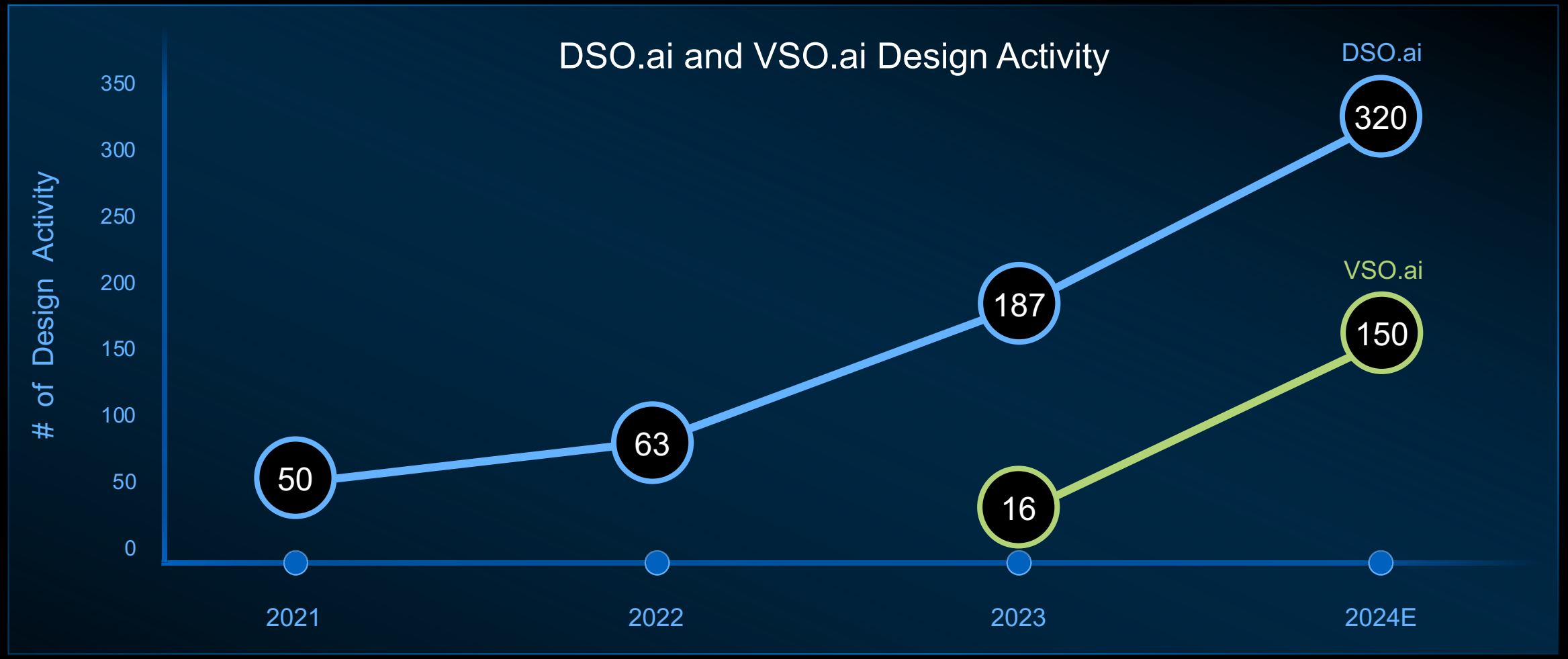
HPC	2X Tests Reduction	Automotive SoC	15% Coverage Boost	CPU	2X Faster TAT

Based on results from deployments at:

AMD intel MEDIATEK Microsoft NVIDIA RENESAS SAMSUNG SONY life.augmented

SYNOPSYS®

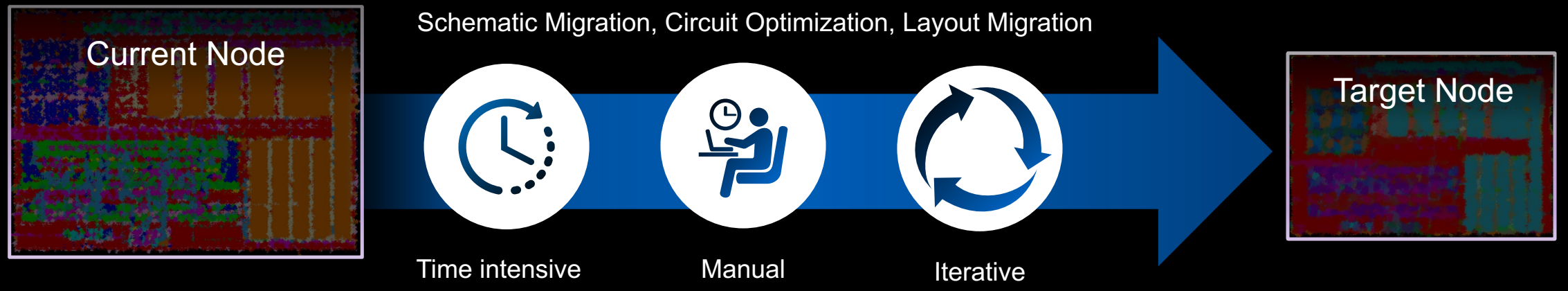
Rapid Adoption of AI-Driven Optimization



AMD intel MEDIATEK Microsoft NVIDIA RENESAS SAMSUNG SONY life.augmented

SYNOPSYS®

Accelerating Analog Migration with ASO.ai



Accelerating Analog Migration with ASO.ai

3x Overall TAT

Improvement

Accelerating Analog Migration with ASO.ai

3x Overall TAT
Improvement

ASO.ai
Faster Time to Results

10x Faster TAT
Analog Circuit Optimization

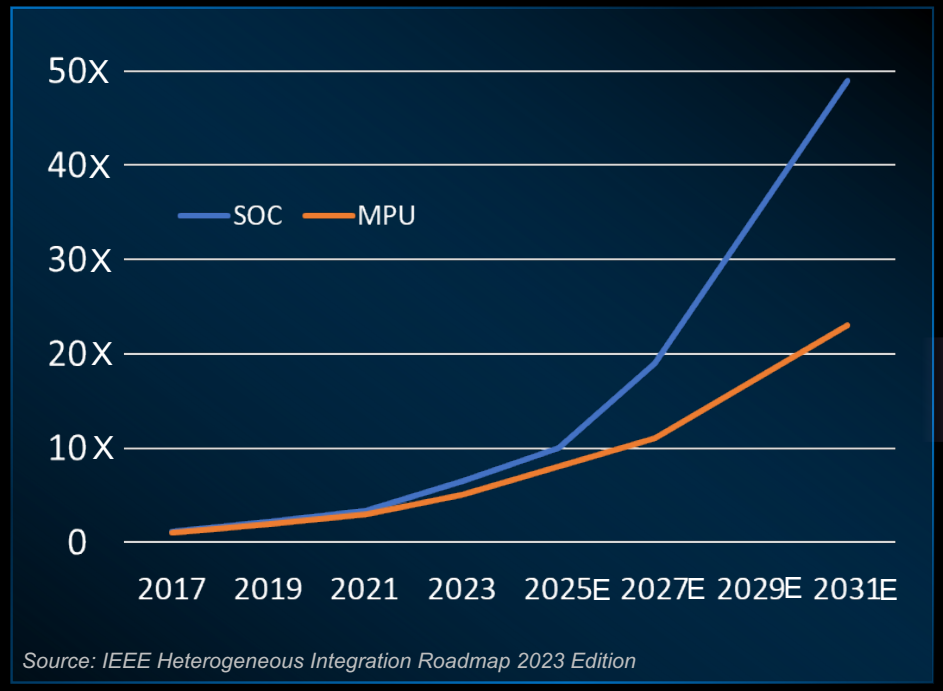
3x Faster TAT
Analog IP Node Migration

Enabled at Leading Foundries

intel SAMSUNG tsmc

TSO.ai Lowers Cost of Testing a Chip

Exponential Growth in Test Times



Source: IEEE Heterogeneous Integration Roadmap 2023 Edition

Die test time directly proportional to test pattern count

TSO.ai

Customer Results
(Pattern Count Reduction)

Mobile	45% - 70%
Systems	18% - 60%
Graphics	19% - 25%

LLM-Based EDA (GenAI) is a New Growth Opportunity

Answer expert questions on tools & workflows

In-context Analysis & Design Debug

Prescriptive Guidance & Workflow recommendation

Design Collateral Gen: RTL, Testbench, Assertion creation

"30% faster ramp-time for junior engineers without having to depend on expert engineers"

"We can focus on the critical tasks while GenAI is taking care of the mundane stuff"

"The responses are at least 2x faster to expert queries than the search process"

AMD intel Microsoft

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Pioneering Innovations Unleash New Growth Vectors

Multi-Die

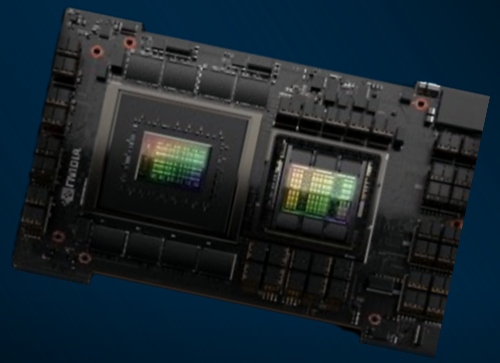
Multi-Die Packages: Enabling Many Transformative Products

AMD
Instinct™ MI300

Gen AI Accelerator
304 GPUs, 192GB HBM3

Source: AMD

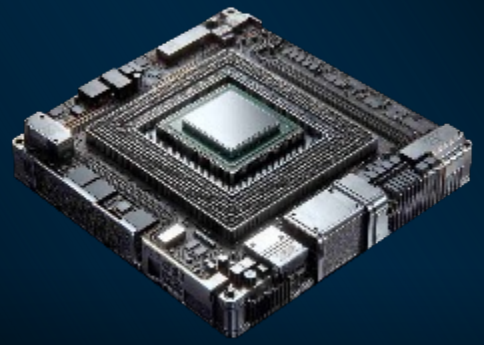
NVIDIA
Grace Hopper



Gen AI Superchip
72-core CPU, H100 Tensor GPU,
96GB HBM3 / 144GB HBM3e

Source: nVIDIA

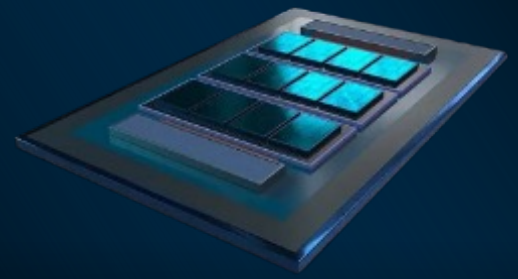
Google
TPU v5



“Hypercomputer” AI
256 chips/pod, 95GB HBM2e

Source: Google

Intel
Clearwater Forest
(Xeon)



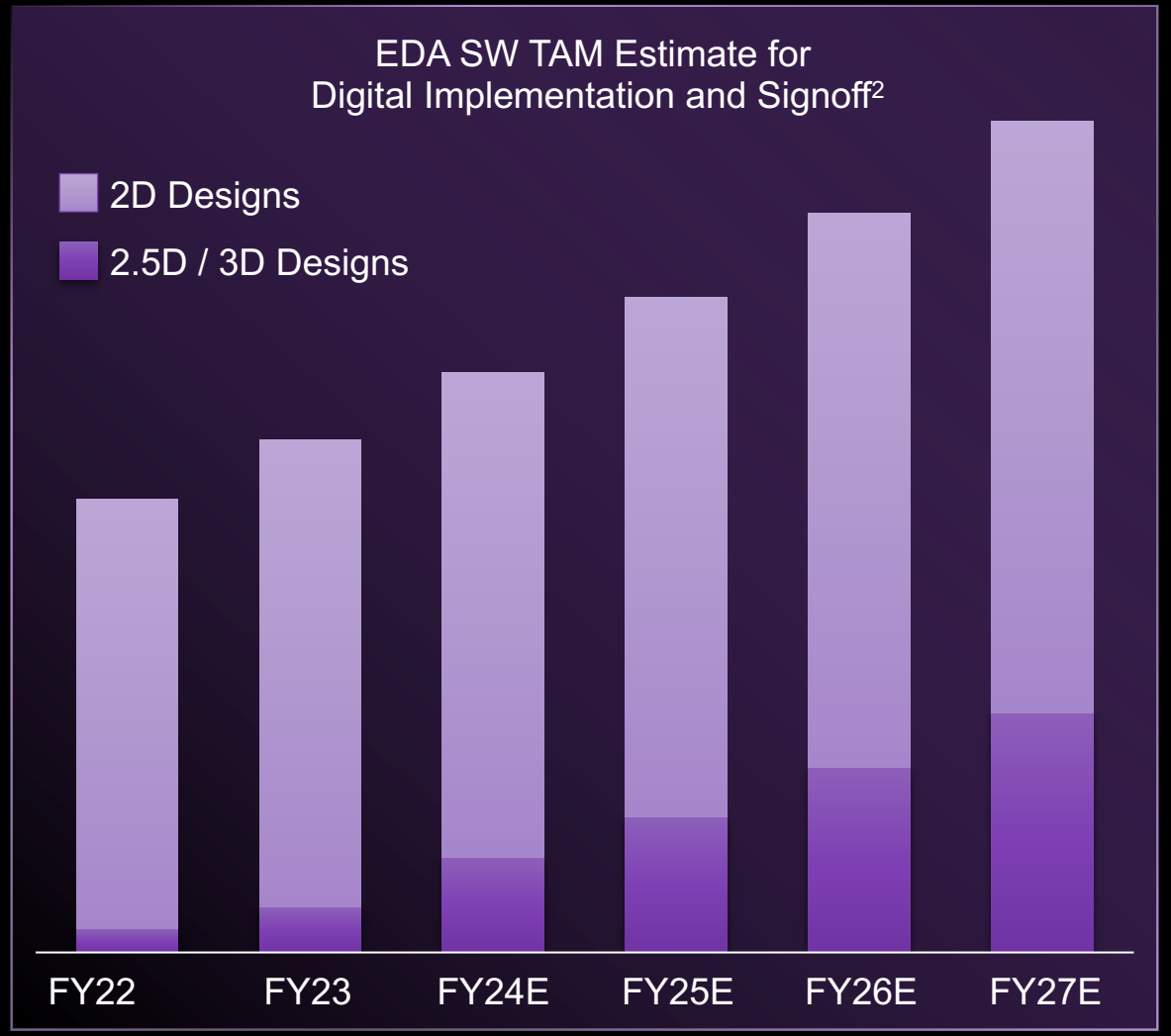
Nextgen Server Chip
288-core CPU, Intel 18A,
Advanced 3D packaging

Source: Intel

Estimated 30% of EDA SW TAM Driven by Multi-Die by 2027

Multi-die Migration Forecast[1]

	By 2027
Server/AI	~90%
PC/Client	~70%
Consumer systems	~10%
Automotive	~10%

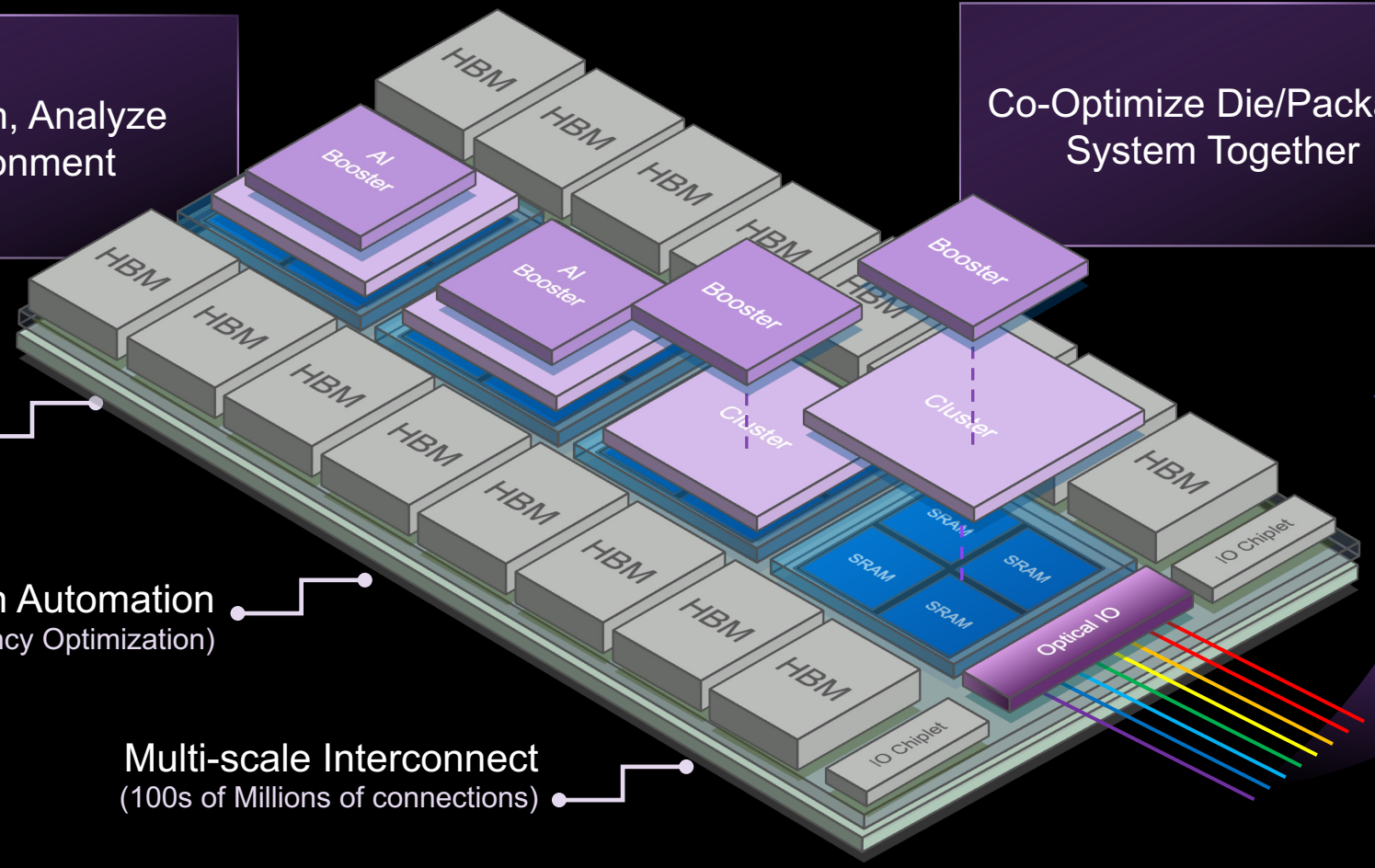


1. *Source: Yole*
2. *Synopsys internal EDA SW TAM modeled for Digital Implementation & Signoff*

Chip-Up Disruption to Meet Trillion-Scale Multi-Die Challenge

Explore, Design, Analyze in one environment

Co-Optimize Die/Package System Together



Chip-Up Disruption

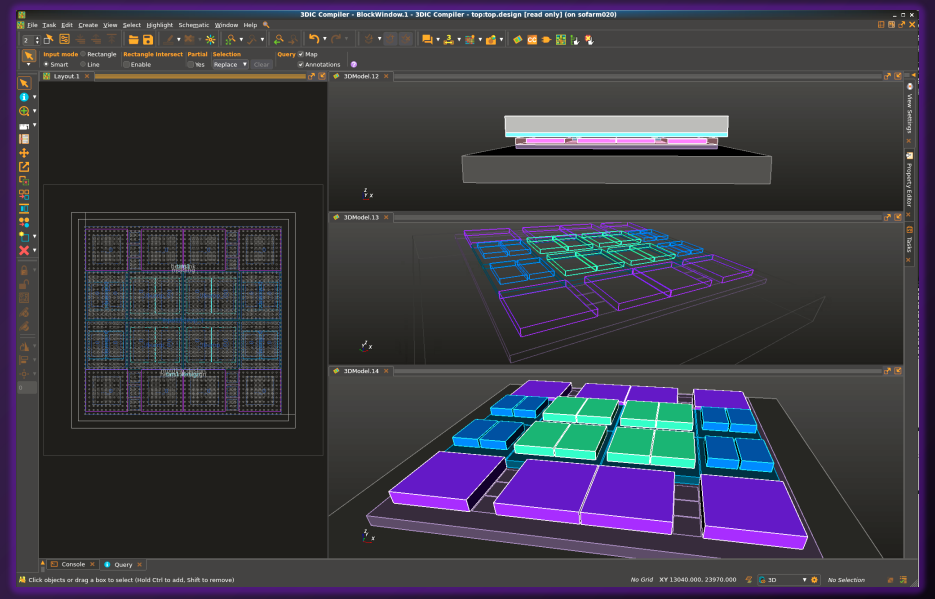
2D/3D-stacked Chiplets
(10s of dies,100Bx Transistors)

HBM Design & Integration Automation
(Bandwidth/Latency Optimization)

Multi-scale Interconnect
(100s of Millions of connections)

Comprehensive Multi-Die Package Solution

Synopsys
3DIC Compiler Platform



Unified Exploration to Signoff
(Common Fusion Data-model and UX)

AI-Powered architecture exploration and design
with software co-development and validation

Broadest Die-to-Die IP portfolio
on silicon-proven technologies

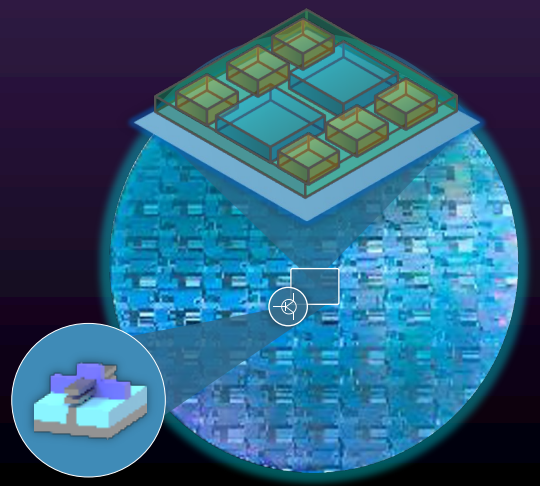
Industry's only unified and scalable platform
for 3D heterogeneous integration design

Integrated Test and Silicon lifecycle management
to improve yield, health and reliability

Enabling Multi-Die Innovation at Market Makers

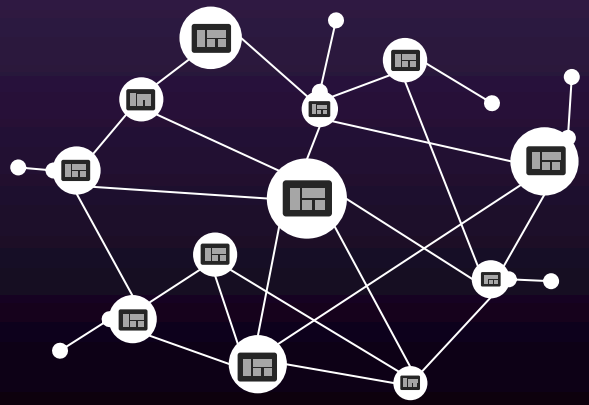
CPU Company

Delivered A^{o} architecture intricacy with 3D integration for 300B+ transistor system



HPC / AI Semi Company

Made over 10 different pieces of silicon to behave as a single superchip



"Single" chip system for AI workloads

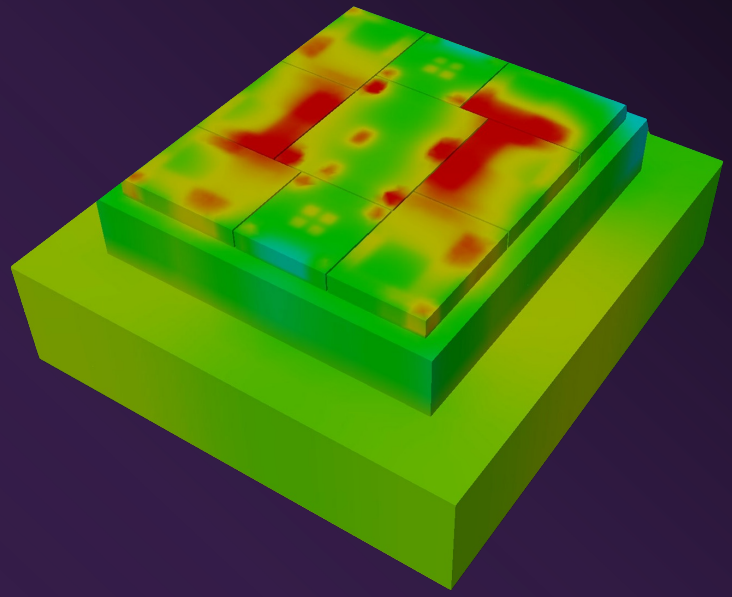
Hyperscale System Company

Optimized thermal profiles to unlock significant energy efficiency

10,000x/more efficiency across the array of datacenter racks of chips

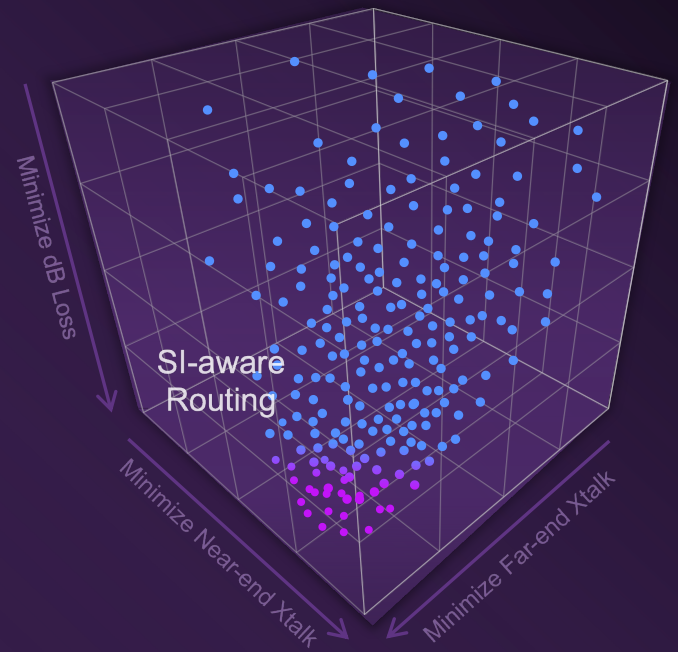
New Innovations to Accelerate Multi-Die Exploration/Design

Fast Native Thermal Analysis



Hours vs. Days
in Incremental Analysis

3DSO.ai: AI-Driven Optimization



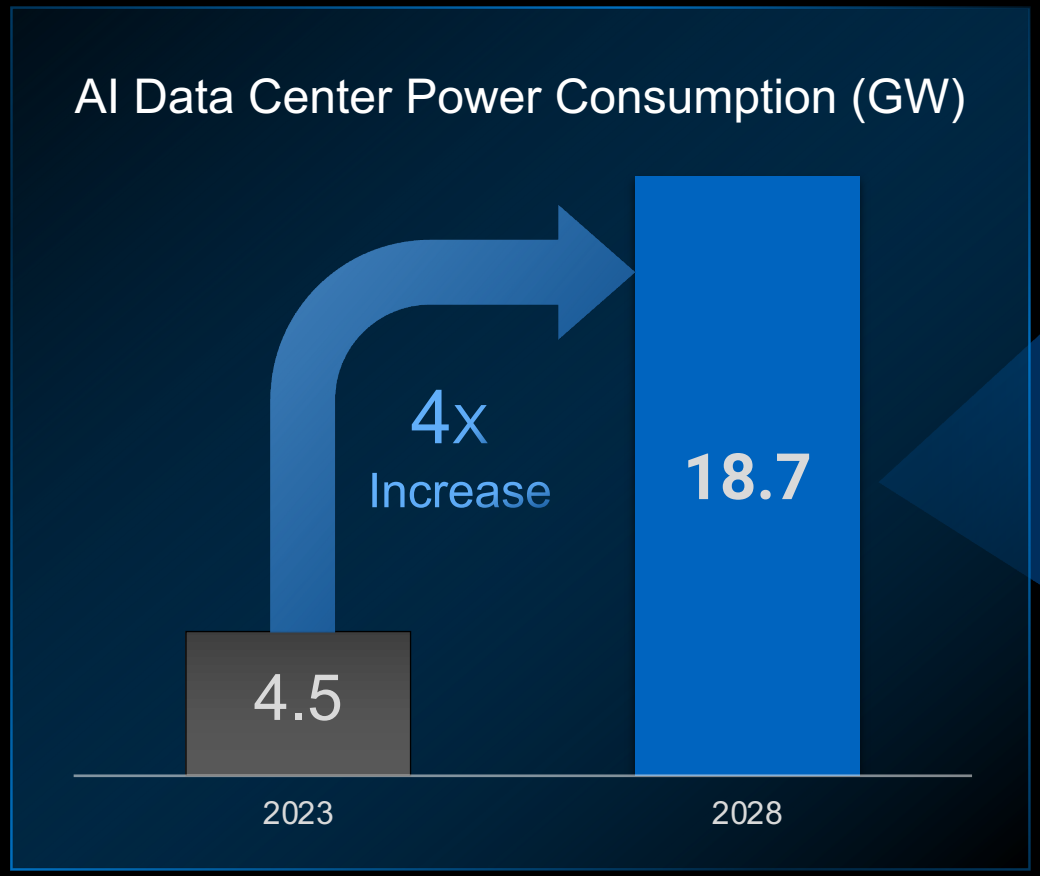
10x Productivity Boost
Superior QoR

SYNOPSYS®

Pioneering Innovations Unleash New Growth Vectors

Energy Efficiency

AI Driving Unprecedented Power Consumption



Source: Schneider Electric, December 2023

nVIDIA H100 GPU

700 Watts*

Source: Schneider Electric, December 2023 ** Thermal Design Power*

Energy to train GPT-4

50 GWh

Source: RISE Research Institutes of Sweden, Oct 2023

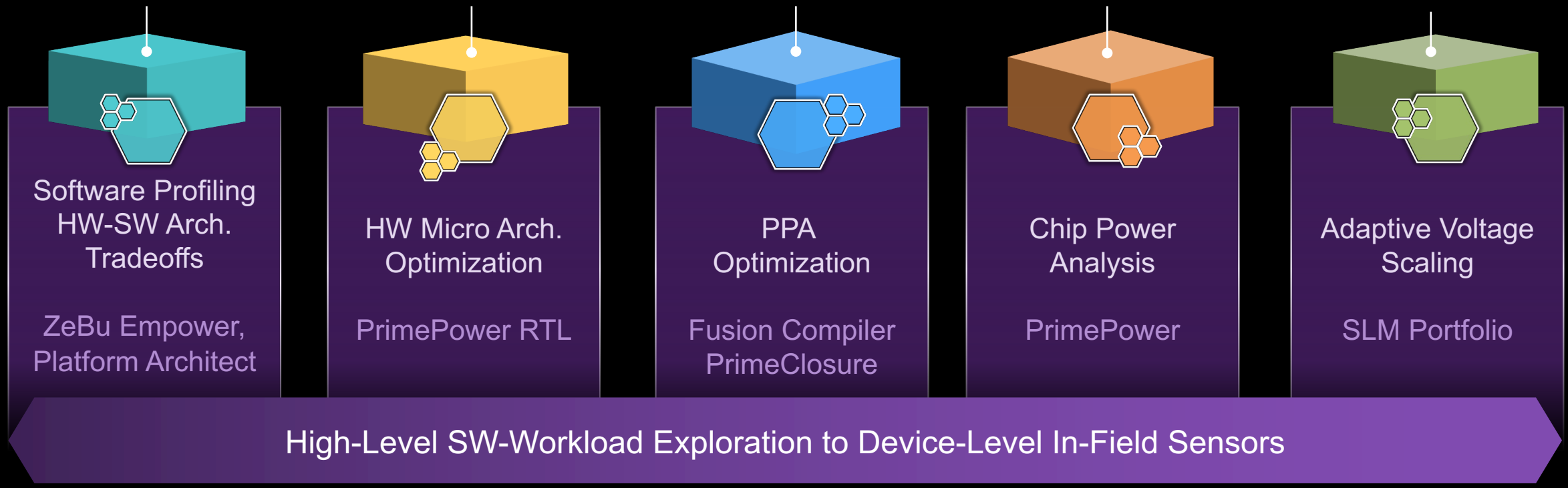
ChatGPT request vs Google search

10x More Power

Source: International Energy Agency, January 2024 report

Software to Device Solution Needed to Address the Magnitude of Power Consumption

Optimizing Power at Every Design Phase



>2x

Savings with Arch. Exploration and SW Profiling of AI Design

20%

Savings from RTL Changes of NPU Design

12%

Dynamic Power Savings from Implementation Opt. of HPC Design

SYNOPSYS®

Pioneering Innovations Unleash New Growth Vectors

EDA Compute Acceleration

EDA Compute Acceleration Innovations

Multi Core

Rapid Transition to 96, 128 Cores

10x TAT for Timing

Signoff on 64 Cores

Distributed

Distributed Computing with 100s of Machines

Near-Linear Acceleration

of Formal Verification

Synopsys EDA

Cloud

Elastic, Scalable Computing on Cloud

In 24 Hours

Physical Verification of Reticle-Limit Chips

GPU

Acceleration of Specific Workloads

GPU Acceleration

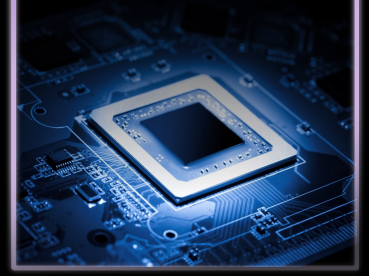
For SPICE, OPC…

SYNOPSYS: MISSION CRITICAL FOR NVIDIA SILICON SUCCESS

DECADES OF COLLABORATION ACROSS FULL EDA SUITE POWERS ACCELERATED COMPUTING

13x Verification

Functional Verification



- Synopsys VCS
- NVIDIA L40
- NVIDIA Grace Hopper

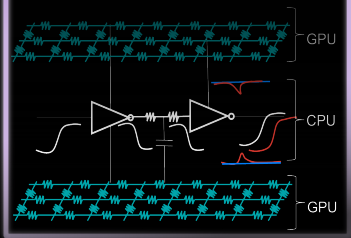
10x Design

Place and Route

- Synopsys Fusion Compiler
- NVIDIA Grace Hopper

15x Simulation

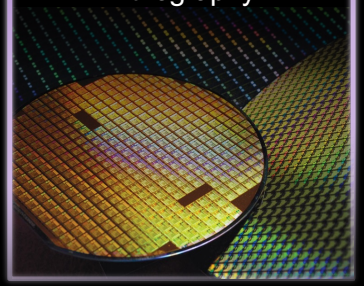
SPICE Simulation



- Synopsys PrimeSim
- NVIDIA Hopper
- NVIDIA Grace Hopper

15x Manufacturing

Computational Lithography



- Synopsys Proteus
- NVIDIA cuLitho
- NVIDIA Grace Hopper

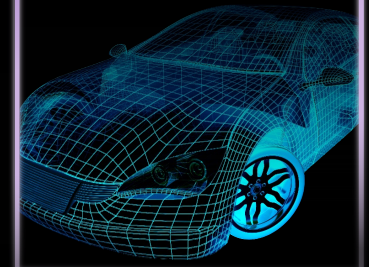
Generative AI

Industry's 1st LLM-Based GenAI EDA Solution

- Synopsys.ai
- NVIDIA NeMo & NIM
- NVIDIA DGX

Systems Software

Testing & Validation of Automotive Software



- Synopsys Electronics Digital Twin, vECU, TPT
- NVIDIA Omniverse

SYNOPSYS® *Performance Speed-Up Based on Projected Results

SYNOPSYS® | NVIDIA

SYNOPSYS: MISSION CRITICAL FOR NVIDIA SILICON SUCCESS

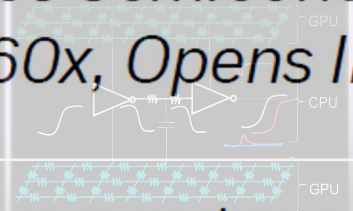
DECADES OF COLLABORATION ACROSS FULL EDA SUITE POWERS ACCELERATED COMPUTING

NVIDIA

TSMC and Synopsys Bring Breakthrough NVIDIA Computational Lithography Platform to Production

Verification	Design	Simulation	Manufacturing	Generative AI	Systems Software
Functional Verification	Place and Route	SPICE Simulation	Computational Lithography	Industry's 1st LLM-Based GenAI EDA Solution	Testing & Validation of Automotive Software

NVIDIA cuLitho Accelerates Semiconductor Manufacturing's Most Compute-Intensive Workload by 40-60x, Opens Industry to New Generative AI Algorithms



"Computational lithography is a cornerstone of chip manufacturing," said Jensen Huang, founder and CEO of NVIDIA. "Our work on cuLitho, in partnership with TSMC and Synopsys, applies accelerated computing and generative AI to open new frontiers for semiconductor scaling."

• Synopsys VCS • NVIDIA Grace Hopper	• Synopsys Fusion Compiler • NVIDIA Grace Hopper	• Synopsys PrimeSim • NVIDIA Grace Hopper	• Synopsys Proteus • NVIDIA Grace Hopper	• Synopsys.ai • NVIDIA DGX	• Synopsys Electronics Digital Twins vECU, TRT • NVIDIA Omniverse

*Performance Speed-Up Based on Projected Results

Synopsys EDA is Mission Critical in the Era of Pervasive AI

Well Positioned with Breadth and Depth of Portfolio

Next-Gen Architecture to Rapidly Fuse Electronics & Multi-Physics

Pioneering in Emerging Areas Unleashes New Growth Vectors

SYNOPSYS®

Our Technology, **Your Innovation**™

THANK YOU

Appendix

GAAP to Non-GAAP Reconciliation
Operating Income and Operating Margin

($ in millions)	2020		2021		2022		2023	
	Margin $	Margin %	Margin $	Margin %	Margin $	Margin %	Margin $	Margin %
GAAP operating income and operating margin	$620.1	16.8%	$734.8	17.5%	$1,162.0	22.9%	$1,269.3	21.7%
Adjustments:								
Amortization of intangible assets	$91.3	2.5%	$82.4	2.0%	$96.7	1.9%	$102.9	1.8%
Stock compensation	$248.6	6.7%	$345.3	8.2%	$459.0	9.0%	$563.3	9.6%
Acquisition-related items	$14.1	0.4%	$15.4	0.4%	$14.1	0.3%	$15.1	0.3%
Restructuring charges	$36.1	1.0%	$33.4	0.8%	$12.1	0.2%	$77.0	1.3%
Non-qualified deferred compensation plan	$21.5	0.6%	$71.6	1.6%	($68.8)	(1.3%)	$20.5	0.4%
Legal Matters	—	—	($1.5)	(0.0%)	—	—	—	—
Non-GAAP operating income and operating margin	$1,031.6	28.0%	$1,281.4	30.5%	$1,675.1	33.0%	$2,048.0	35.1%
Non-GAAP operating margin expansion FY20–FY23								7.1% / 706bps

GAAP to Non-GAAP Reconciliation
Net Income per Diluted Share

	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
GAAP net income per diluted share	**$1.56**	**$1.47**	**$1.21**	**$1.58**	**$1.64**	**$1.43**	**$1.73**	**$0.88**	**$2.82**	**$3.45**	**$4.27**	**$4.81**	**$6.29**	**$7.92**
Adjustments:														
Amortization of intangible assets	$0.31	$0.46	$0.66	$0.81	$0.80	$0.86	$0.84	$0.70	$0.82	$0.65	$0.59	$0.52	$0.61	$0.64
Stock compensation	$0.40	$0.38	$0.48	$0.43	$0.51	$0.54	$0.63	$0.70	$0.91	$1.01	$1.60	$2.19	$2.93	$3.62
Acquisition-related items	$0.14	$0.01	$0.30	$0.04	$0.04	$0.10	$0.07	$0.06	$0.14	$0.04	$0.08	$0.10	$0.06	$0.10
In-process research and development	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Inventory fair value adjustment	–	–	$0.01	$0.04	–	–	–	–	–	–	–	–	–	–
Restructuring charges	$0.01	–	–	–	$0.00	$0.10	$0.06	$0.24	$0.08	$0.31	$0.23	$0.21	$0.08	$0.50
Gain on sale of strategic investments	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Tax adjustments and settlement	($0.82)	($0.52)	($0.55)	($0.46)	($0.35)	($0.22)	($0.31)	$0.79	($1.03)	($0.78)	($1.22)	($0.98)	($1.07)	($1.59)
Legal Matters	–	–	–	–	($0.11)	($0.04)	–	$0.05	$0.17	($0.12)	$0.00	($0.01)	–	–
Non-GAAP net income per diluted share	**$1.60**	**$1.80**	**$2.10**	**$2.44**	**$2.53**	**$2.77**	**$3.02**	**$3.42**	**$3.91**	**$4.56**	**$5.55**	**$6.84**	**$8.90**	**$11.19**
Non-GAAP EPS CAGR (FY10-20)											**13%**			
Non-GAAP EPS CAGR (FY20-23)														**26%**

Reconciliation of Unlevered Free Cash Flow and Related Metrics

($ in millions)	**FY2020**	**FY2021**	**FY2022**	**FY2023**
Cash flow from operating activities	$991	$1,493	$1,739	$1,703
(-) Purchases of Property and Equipment	(155)	(94)	(137)	(190)
(-) Capitalized Software Development Costs	(4)	(2)	(2)	(2)
= Free Cash Flow	$832	$1,397	$1,600	$1,511
(/) Revenue	$3,685	$4,204	$5,082	$5,843
= Free Cash Flow Margins	22.6%	33.2%	31.5%	25.9%
Free Cash Flow Margin expansion FY20–FY23				3.3% / 330bps

Business Segment Reporting[1, 2]

UNAUDITED, IN MILLIONS

	FY 2021	FY 2022	FY 2023
Revenue by segment			
Design automation	$2,754.7	$3,300.2	$3,775.3
% of total	65.5%	64.9%	64.6%
Design IP	$1,055.7	$1,315.5	$1,542.7
% of total	25.1%	25.9%	26.4%
Software integrity	$393.8	$465.8	$524.6
% of total	9.4%	9.2%	9.0%
Adjusted operating income by segment			
Design automation	$924.6	$1,206.6	$1,439.7
Design IP	$318.5	$421.5	$532.1
Software integrity	$38.3	$47.0	$76.3
Adjusting operating margin by segment			
Design automation	33.6%	36.6%	38.1%
Design IP	30.2%	32.0%	34.5%
Software integrity	9.7%	10.1%	14.5%

Certain operating expenses are not allocated to the segments and are managed at a consolidated level. The unallocated expenses managed at a consolidated level, including amortization of intangible assets, stock-based compensation, the gains (losses) related to deferred compensation plan, restructuring charges, and certain acquisition-related items, are presented in the table below to provide a reconciliation of the total adjusted operating income from segments to our consolidated operating income:

1 Synopsys' fiscal year 2023 ended on October 28, 2023. For presentation purposes, we refer to the closest calendar month end

2 Synopsys manages the business on a long-term, annual basis, and considers quarterly fluctuations of revenue and profitability as normal elements of our business. Amounts may not foot due to rounding